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Fonseca UMA Schematics Document

rPGA988A Mobile Arrandale

Intel Ibex Peak-M

2009-11-03

REV : X01

```
DY : Nopop Component
B_TPM:Use Lom TPM
C_TPM:Use China TPM
```

<Core Design>

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Title	Cover Page	
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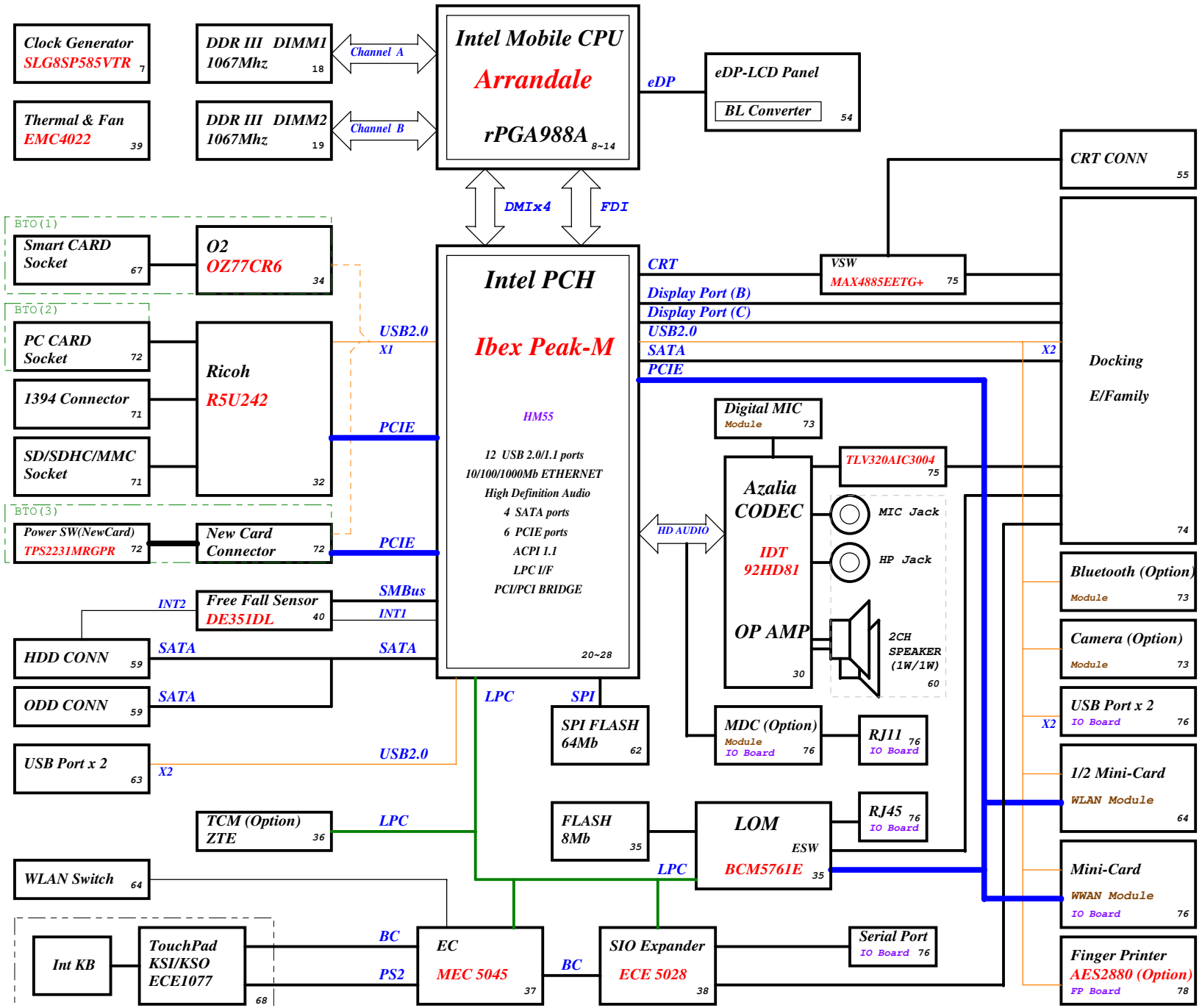
Fonseca UMA Block Diagram

	DF3-14	DF3
Project code	91.4GN01.001	91.4EQ01.001
PCB P/N	48.?????.0SB	48.?????.0SB
Revision	09276 - SB	09226 - SB



CPU DC/DC ISL62883 — 47

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51125 — 46

INPUTS	OUTPUTS
+PWR_SRC	+3.3V_ALW +5V_ALW

SYSTEM DC/DC TPS51116 — 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT

SYSTEM DC/DC TPS51218 — 52

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM LDO RT9035 — 51

INPUTS	OUTPUTS
+3.3V_SUS	+1.8V_RUN

SYSTEM DC/DC ADP3211 — 53

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

BATTERY CHARGER TI BQ24745 — 45
(AC, Battery Existence)

INPUTS	OUTPUTS
+DC_IN_SS	+PBATT

<Core Design>

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Title: Block Diagram

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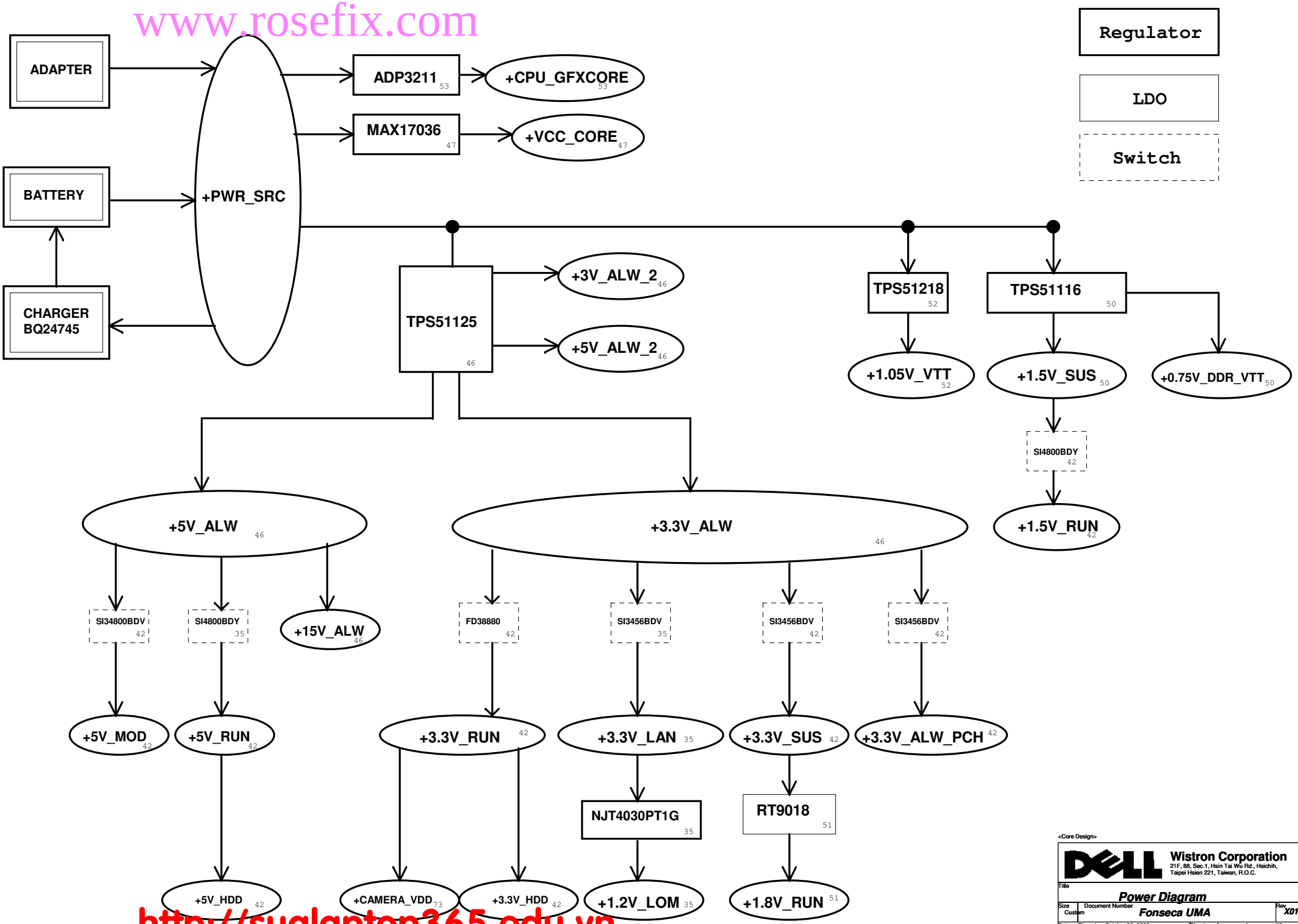

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Title: Power Diagram

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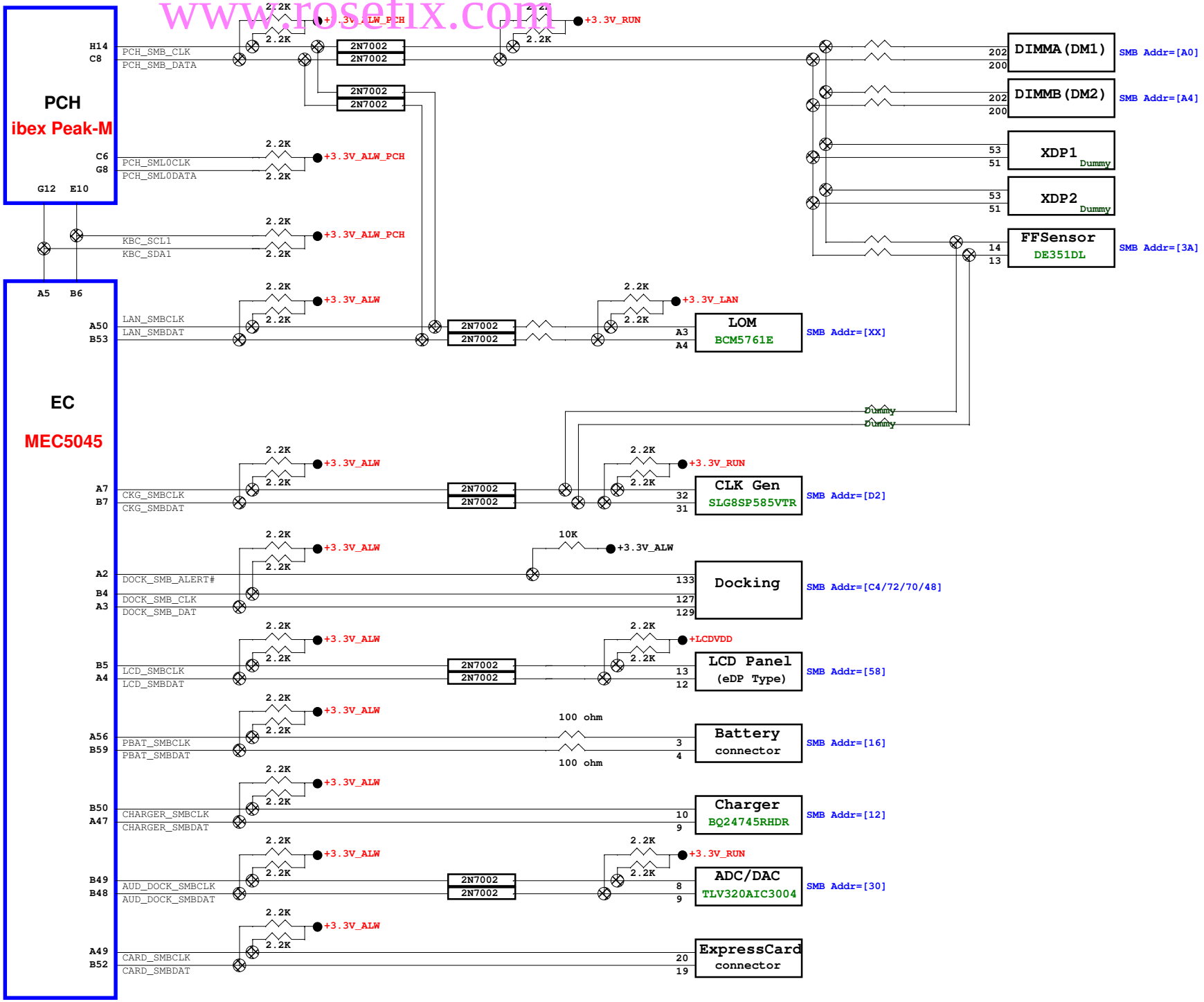

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Title: SMBus Diagram

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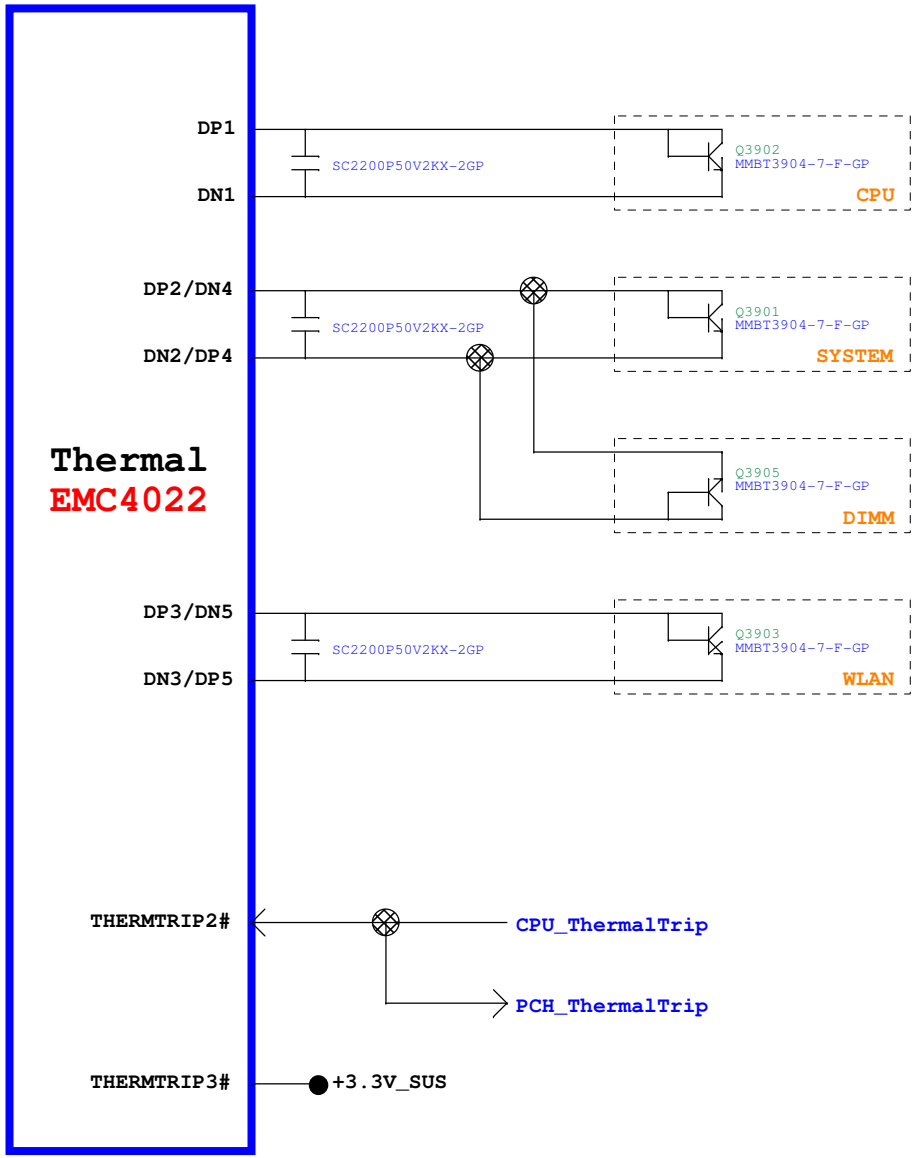
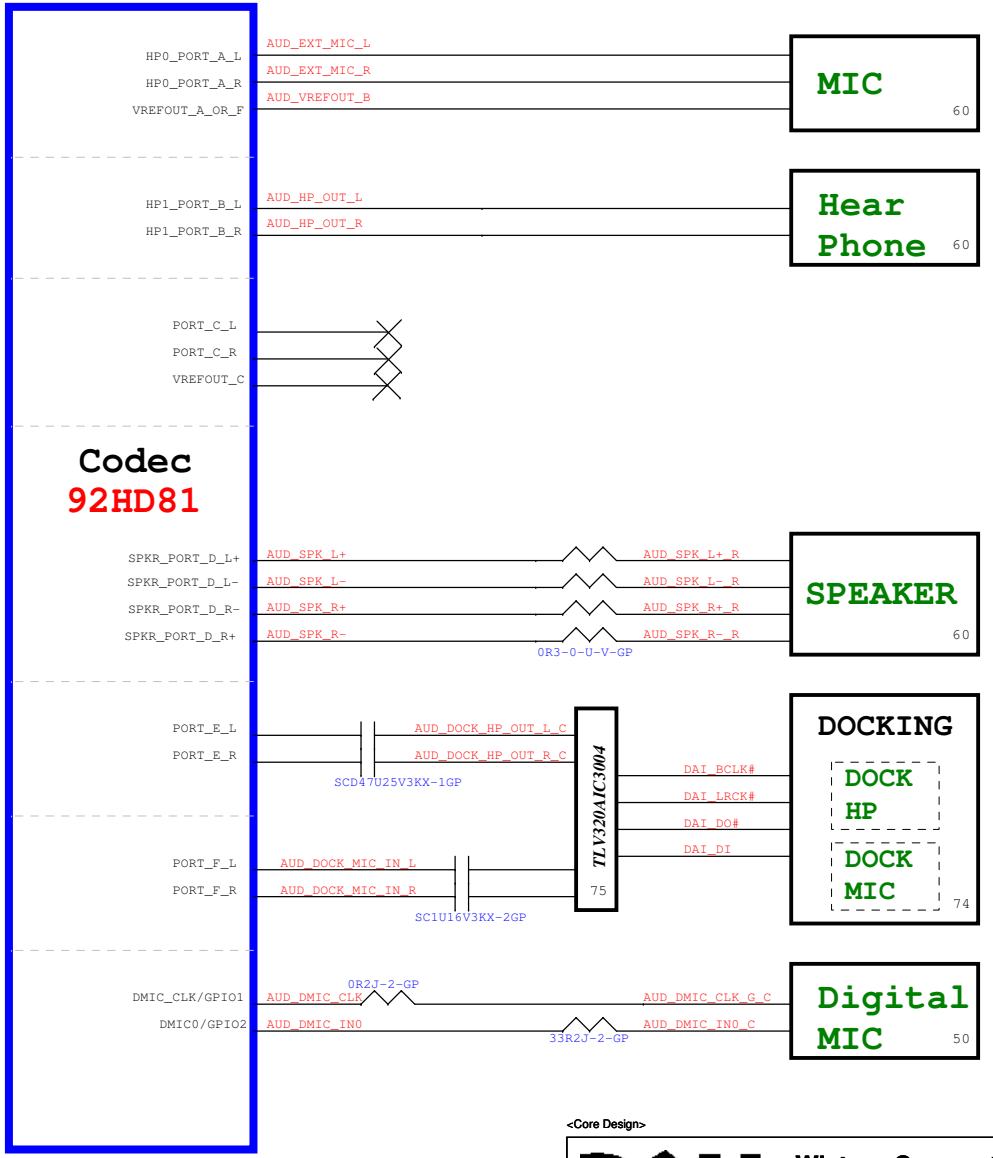
Thermal Block Diagram



Audio Block Diagram



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Title: AUDIO/THERMAL Diagram

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PCH Strapping

Calpella Schematic Checklist Rev: 1.6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** **Note:** Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ ; do not stuff resistor
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-k resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default –** Internal pull-up. **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:** Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:** Connect to +NVRAM_VCCQ with 8.2-kΩ weak pull-up resistor [CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:** Leave floating (internal pull-down).
NV_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1):** Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:** CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) – Intel ME Crypto Transport Layer Security TLS) cipher suite with no confidentiality. High (1) – Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1K pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default =** Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev: 1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1

PCIE Routing

LANE1	WWAN
LANE2	WLAN
LANE3	PCMCIA
LANE4	Express Card
LANE5	None
LANE6	10M/100M/1G LAN
LANE7	**Not available for HM55**
LANE8	**Not available for HM55**

USB Routing

USB	
Pair	**Device**
0	**USB0 @ MB**
1	**USB1 @ MB**
2	**USB2 @ IO Board**
3	**USB3 @ IO Board**
4	**WLAN**
5	**Bluetooth**
6	**Not available for HM55**
7	**Not available for HM55**
8	**DOCKING PORT1**
9	**DOCKING PORT2**
10	**Finger Printer**
11	**Camera**
12	**PCCard / SmartCard**
13	**WWAN**

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Title: *Table of Content*

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SSID = CLOCK

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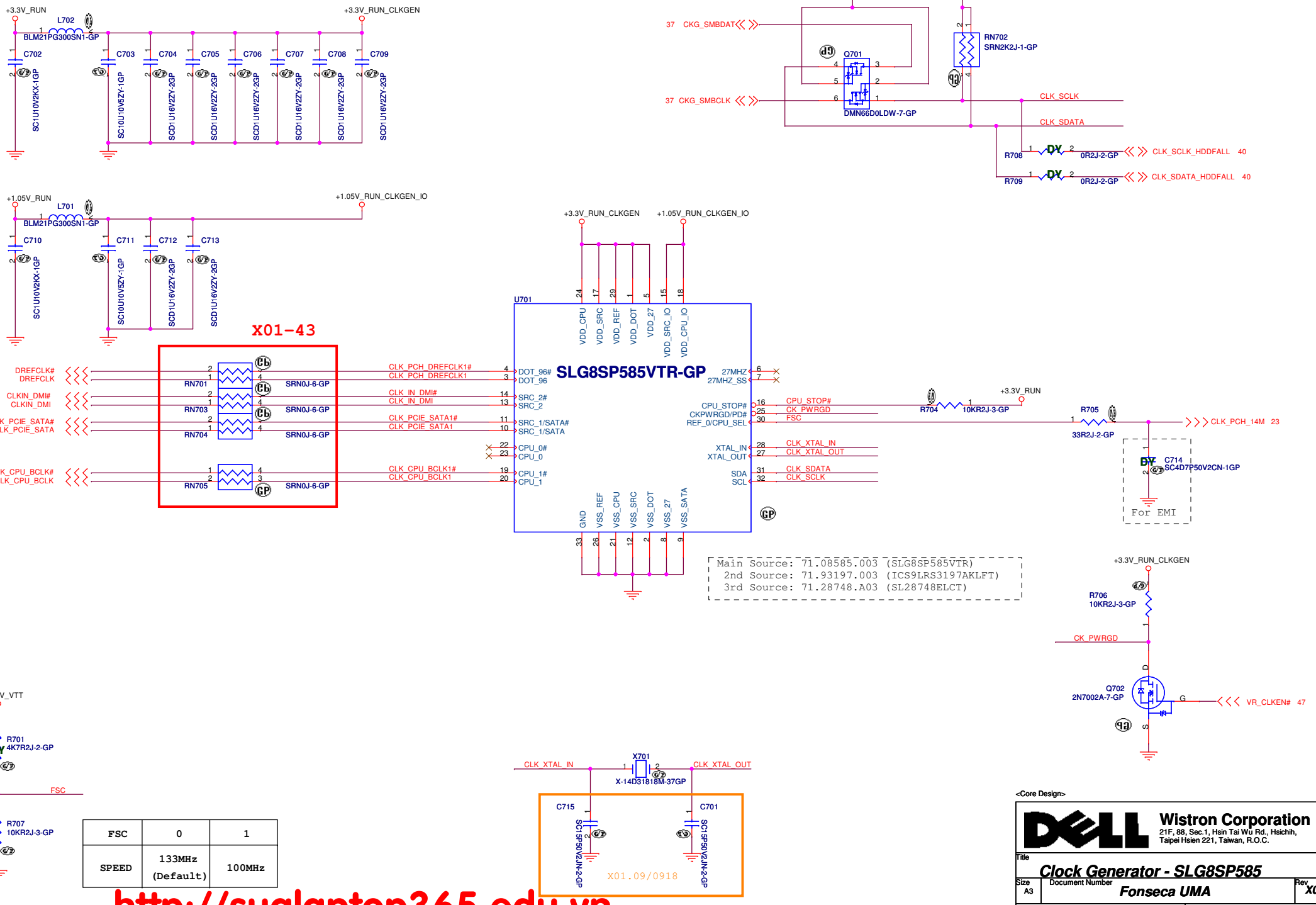

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator - SLG8SP585

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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SSID = CPU
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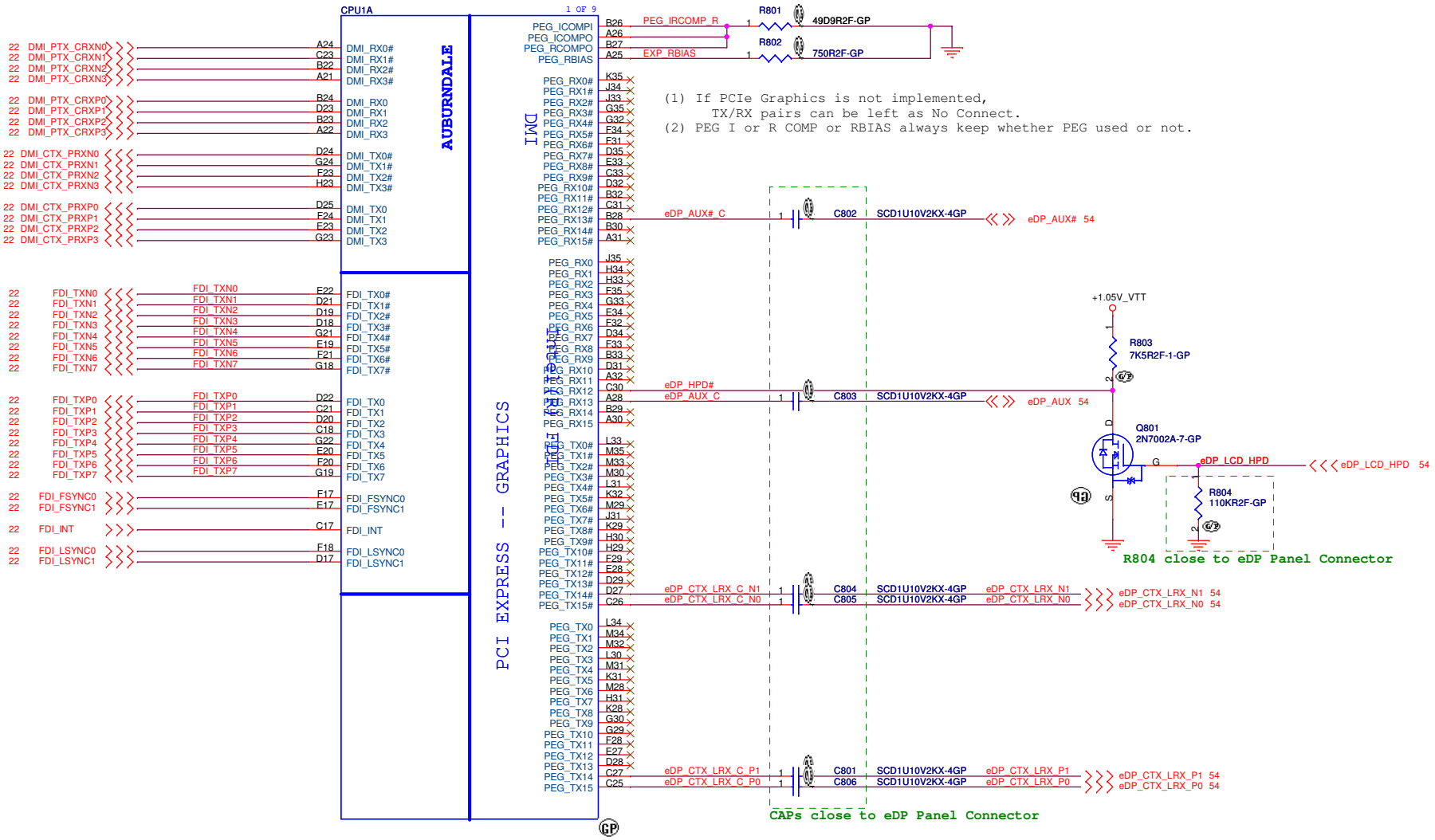

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Title: CPU - PCIE/DMI/FDI (1/7)

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SSID = CPU

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X01-43

Processor Pullups

Processor Compensation Signals

DDR3 Compensation Signals

JTAG MAPPING

X01-4

Scan Chain (Default)	Stuff --> R929, R901, R932 No Stuff --> R930, R931
CPU Only	Stuff --> R929, R930 No Stuff --> R901, R931, R932
GMCH Only	Stuff --> R931, R932 No Stuff --> R929, R930, R901

<Core Design>

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Title: CPU Thermal/Clock/PM (2/7)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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SSID = CPU

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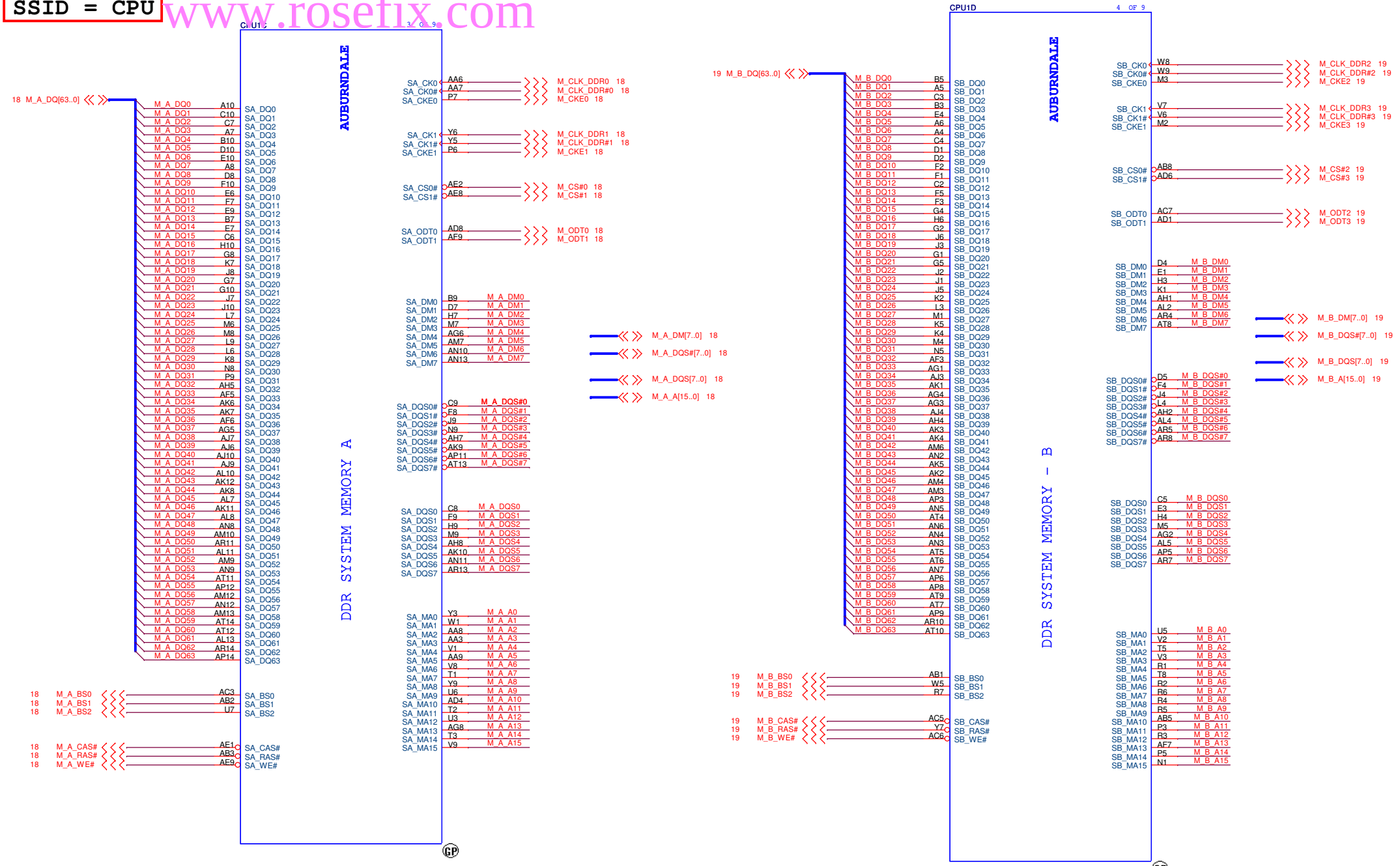

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Title: CPU - DDR (3/7)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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SSID = CPU

SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor

CPU1E — 5 OF 9 — AUBURNDALE

TP1115	VREF_CH_A_DIMM	AP25	RSVD#AP25
TP1116	VREF_CH_B_DIMM	AL25	RSVD#AL25
		AL24	RSVD#AL24
		AL22	RSVD#AL22
		AJ33	RSVD#AJ33
		AG9	RSVD#AG9
		M27	RSVD#M27
		L28	RSVD#L28
		J17	SA_DIMM_VREF#
		H17	SB_DIMM_VREF#
		G25	RSVD#G25
		G17	RSVD#G17
		E31	RSVD#E31
		E30	RSVD#E30

		AJ13	RSVD#AJ13
		AJ12	RSVD#AJ12
		AH25	RSVD#AH25
		AK26	RSVD#AK26
		AL26	RSVD#AL26
		AR2	RSVD_NCTF#AR2
		AJ26	RSVD#AJ26
		AJ27	RSVD#AJ27

H_RSVD32 — TP1118; H_RSVD33 — TP1117; H_RSVD35 — TP1119; H_RSVD36 — TP1120

CPU Piin AJ13 and AJ12:
Core voltage sense line.
Via from PGA pad to the back of the MB and provide test point.
Do not route any additional trace.

TP1101	CFG0	AM30	CFG0
TP1102	CFG1	AM28	CFG1
	CFG2	AP31	CFG2
	CFG3	AL32	CFG3
	CFG4	AL30	CFG4
TP1103	CFG5	AM31	CFG5
TP1104	CFG6	AN29	CFG6
	CFG7	AM32	CFG7
TP1105	CFG8	AK32	CFG8
TP1106	CFG9	AK31	CFG9
TP1107	CFG10	AK28	CFG10
TP1108	CFG11	AJ28	CFG11
TP1109	CFG12	AN30	CFG12
TP1110	CFG13	AN32	CFG13
TP1111	CFG14	AJ32	CFG14
TP1112	CFG15	AJ29	CFG15
TP1113	CFG16	AJ30	CFG16
TP1114	CFG17	AK30	CFG17
		H16	RSVD_TP#H16

RESERVED

		AL28	RSVD#AL28
		AL29	RSVD#AL29
		AP30	RSVD#AP30
		AP32	RSVD#AP32
		AL27	RSVD#AL27
		AT31	RSVD#AT31
		AT32	RSVD#AT32
		AP33	RSVD#AP33
		AR33	RSVD#AR33
		AR32	RSVD#AR32
		E15	RSVD_TP#E15
		F15	RSVD_TP#F15
		A2	KEY
		D15	RSVD#D15
		C15	RSVD#C15
		AJ15	RSVD#AJ15
		AH15	RSVD#AH15
		B19	RSVD#B19
		A19	RSVD#A19
		A20	RSVD#A20
		B20	RSVD#B20
		U9	RSVD#U9
		T9	RSVD#T9
		AC9	RSVD#AC9
		AB9	RSVD#AB9
		AA5	RSVD_TP#AA5
		AA4	RSVD_TP#AA4
		R8	RSVD_TP#R8
		AD3	RSVD_TP#AD3
		AD2	RSVD_TP#AD2
		AA2	RSVD_TP#AA2
		AA1	RSVD_TP#AA1
		R9	RSVD_TP#R9
		AG7	RSVD_TP#AG7
		AE3	RSVD_TP#AE3
		V4	RSVD_TP#V4
		V5	RSVD_TP#V5
		N2	RSVD_TP#N2
		AD5	RSVD_TP#AD5
		AD7	RSVD_TP#AD7
		W1	RSVD_TP#W3
		W2	RSVD_TP#W2
		N3	RSVD_TP#N3
		AE5	RSVD_TP#AE5
		AD9	RSVD_TP#AD9
		J29	RSVD#J29
		J28	RSVD#J28
		AP34	VSS

RSVD_VSS — R1117 0R2J-2-GP

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

CFG0 — R1102 3K01R2F-3-GP (DY)

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled (Clarkfiled only)

CFG3 — R1105 3K01R2F-3-GP (DY)

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 — R1109 3K3R2J-3-GP

X01-47

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7 — R1103 3K01R2F-3-GP (DY)

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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Title: CPU - Reserve (4/7)
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SSID = CPU

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PROCESSOR CORE POWER

48A

AUBURNDALE

6 OF 9

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that
The VTT Rail values are
Arrandale for VTT=1.05V
Clarksfield for VTT=1.1V

Arrandale drives this pin High for 1.05V
Clarksfield drives this pin Low for 1.1V

Place near PU4701

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Title: CPU - VCC_CORE (5/7)

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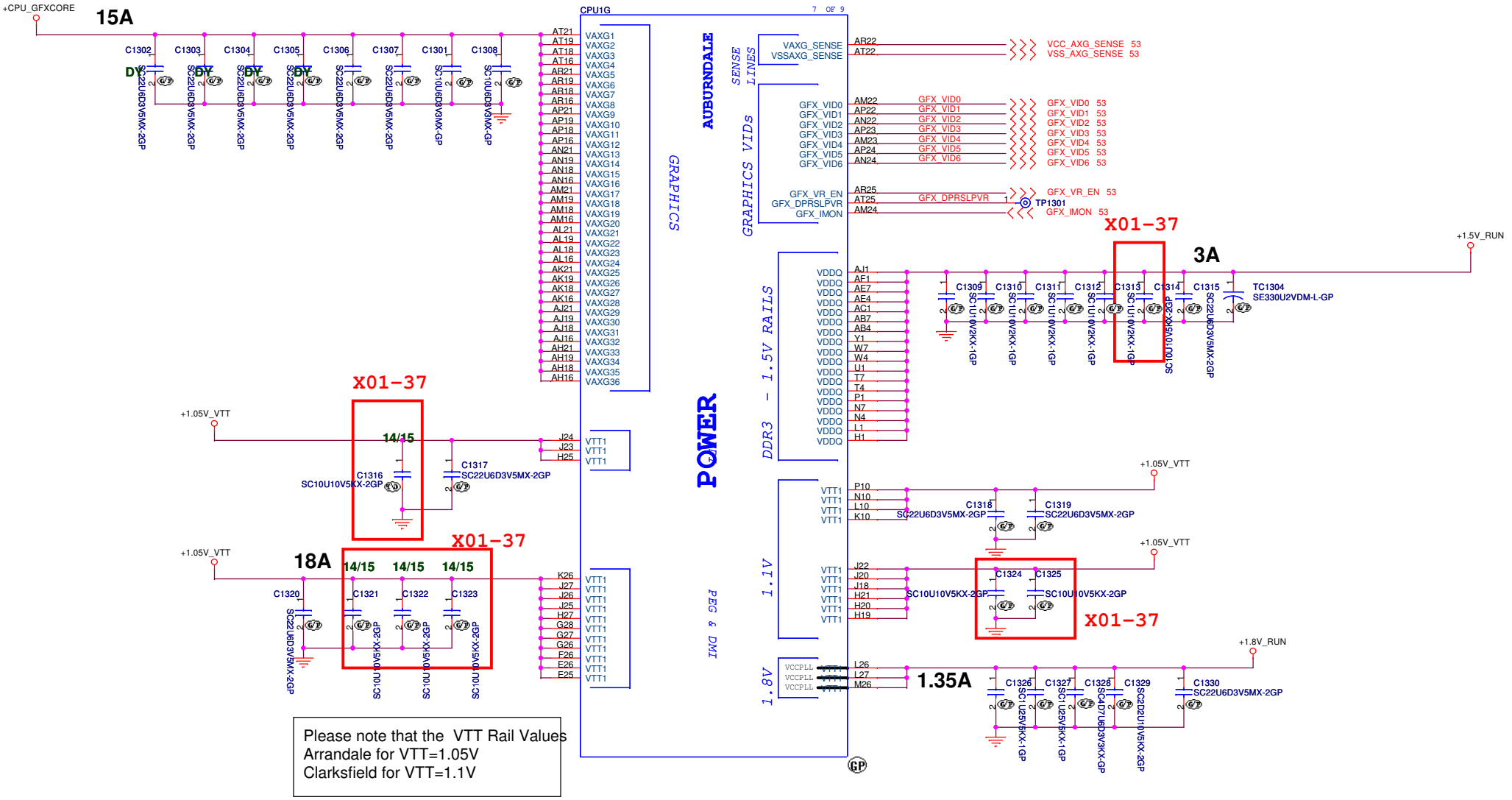

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Title: CPU - GFXCORE (6/7)

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SSID = CPU

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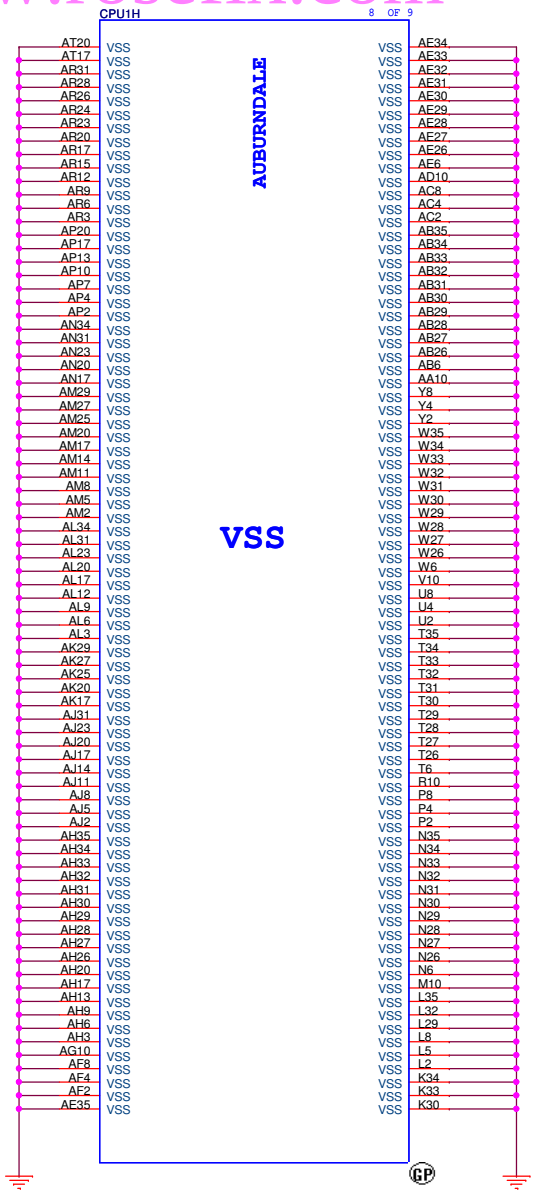

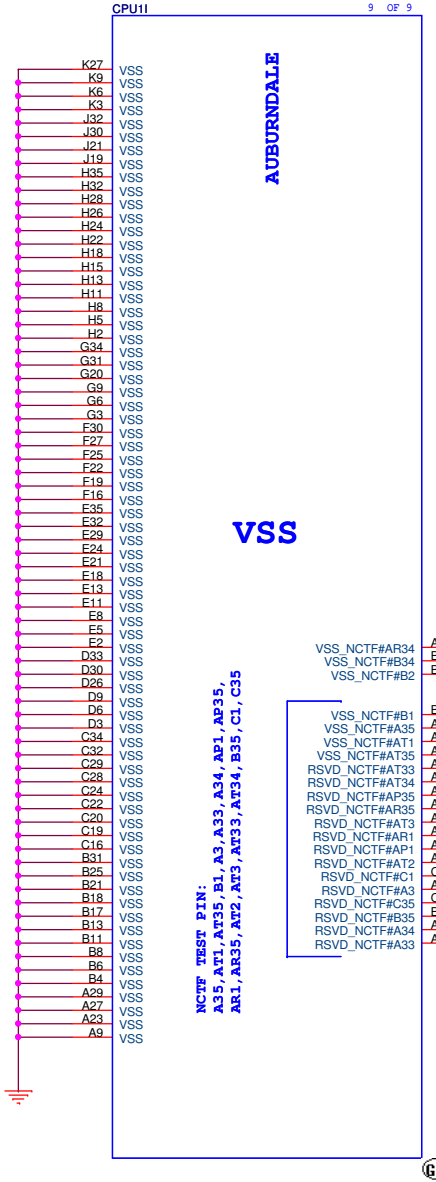

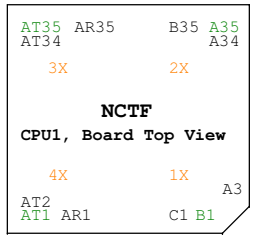

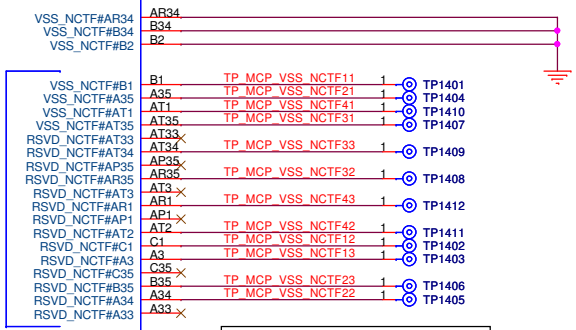

All NCTF pins should be Test Points and should be routed as trace.

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Title: CPU - VSS (7/7)

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Title: Reserve

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SSID = Memory

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SO-DIMMA
H = 9.2mm

DM1

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

SODIMM A DECOUPLING

X01-37

Layout Note:
Place these Caps near SO-DIMMA.

14ONLY

15ONLY

Place between DM1 and DM2.

Place these caps close to VTT1 and VTT2.

Near Memory +1.5V_SUS Plane

Near CPU +1.5V_RUN Plane

Reverse Type

DDR3-204P-42-GP

62.10017.N61

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Title: DDR III Socket - DM1

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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SSID = Memory

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SO-DIMMB
H = 5.2mm

DM2

DDR3-204P-48-GP

Reverse Type

62.10017.P41

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

X01-37

Place these caps close to VTT1 and VTT2.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR III Socket - DM2

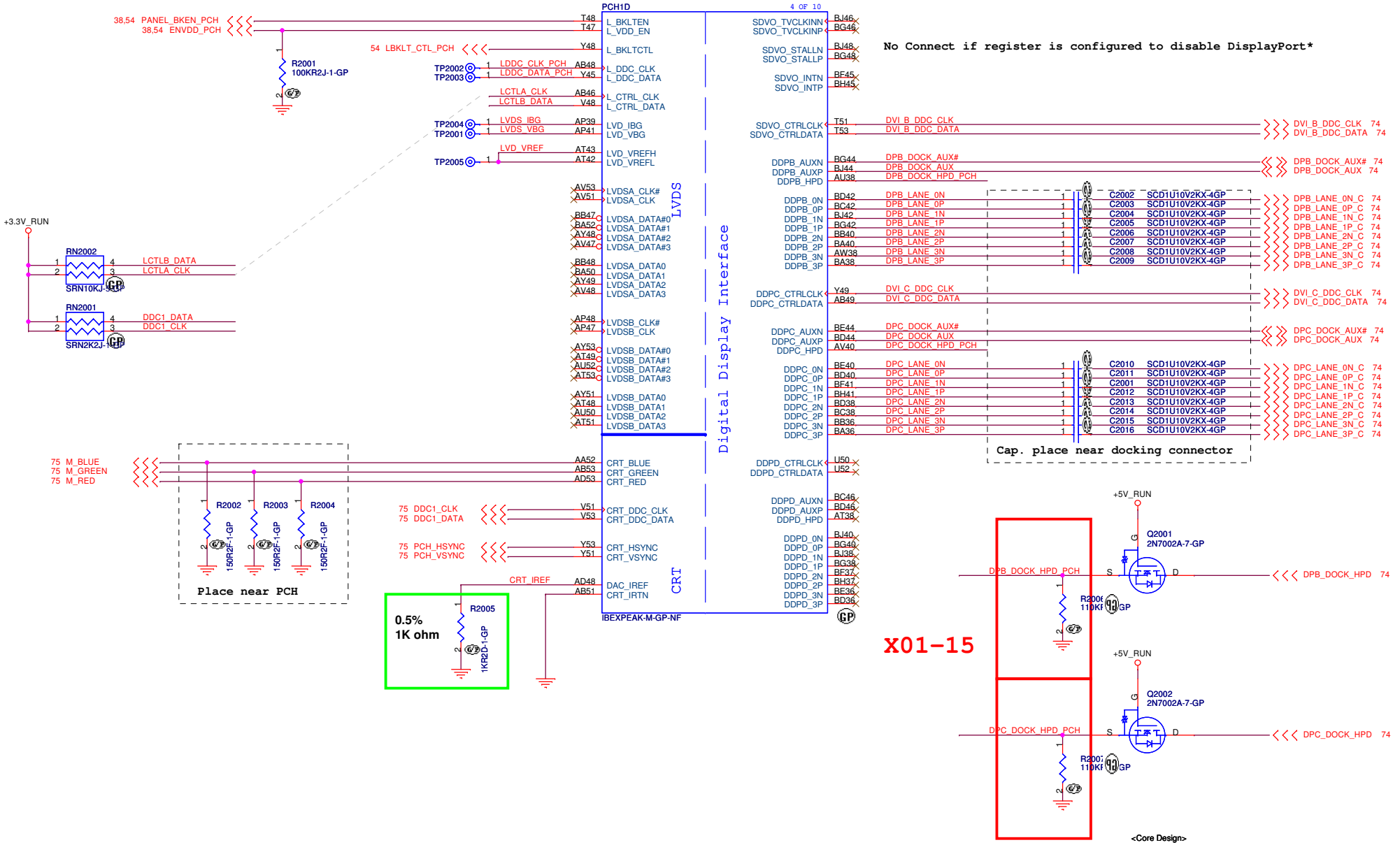
Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 19 of 82

http://sualaptop365.edu.vn

SSID = PCH

www.rosefix.com



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - LVDS/CRT/DDI (1/9)

Size	Document Number	Rev
A3	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 20 of 82

http://sualaptop365.edu.vn

SSID = PCH

www.rosefix.com

Consider layout routing

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:
Disabled when Low.
Enable when High.

USB	
Pair	Device
0	USB0 @ MB (Charger)
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCK1
9	DOCK2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI(Default)

PCI_GNT[3:0]#: Internal pull high during Strap

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - PCI/USB/NVRAM (2/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 21 of 82

SSID = PCH

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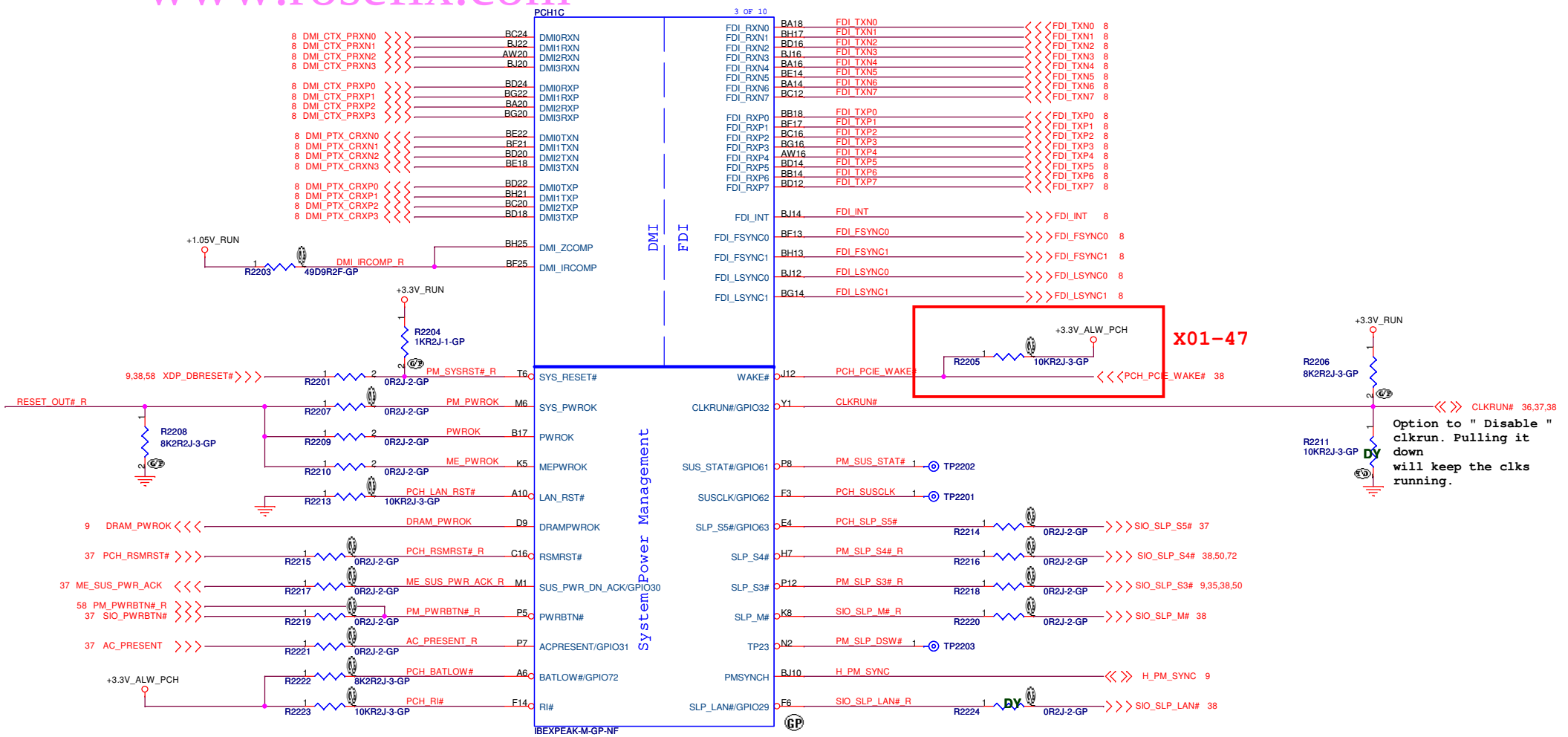

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - DMI/FDI/PM (3/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 22 of 82

http://sualaptop365.edu.vn

SSID = PCH

www.rosefix.com

PCH1B

2 OF 10

IBEXPEAK-M-GP-NF

PCIe port 7 and 8 may not be available for all Ibex Peak SKUs.

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

From Intel DG 1.6
CLKOUTFLEX{3:0}
RS on PCI/NonPCI Routing (for single / double-load)
=> 22 ohm series resistor

X01-43

X01-41

14ONLY

X01-33

15ONLY

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - PCIE/SMBUS/CLOCK/CL (4/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 23 of 82

SSID = PCH

www.rosefix.com

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH1A

1 OF 10

IBEXPEAK-M-GP-NF

X01.09/0918

SRTCRST# new signal Pin

SATA port 2 and 3 may not be available for all Ibex Peak SKUs.

X01-47

X01-30

X01-48

HDD

ODD

DOCKING eSATA

For EMI, RF Cap.

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

Place near PCH side

Form DG1.5
TRST# on PCH does not belong to JTAG interface.
For ES1 silicon, an ext. pull up 3.3-V Sus is required for bias internal state.
A 20-K/10-K voltage divider to this signal to 1.1 V.
However, from ES2 silicon onward, this signal is a No Connect regardless if JTAG interface on PCH is enabled or not.

Pull up +3.3V_M enable iAMT(DY disable)

Internal pull-up of 20K for HDA_DOCK_EN#,

integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH - SPI/RTC/LPC/SATA/IHDA (5/9)

Size	Document Number	Rev
A3	Fonseca UMA	X01

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20.F1000.003

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SSID = PCH

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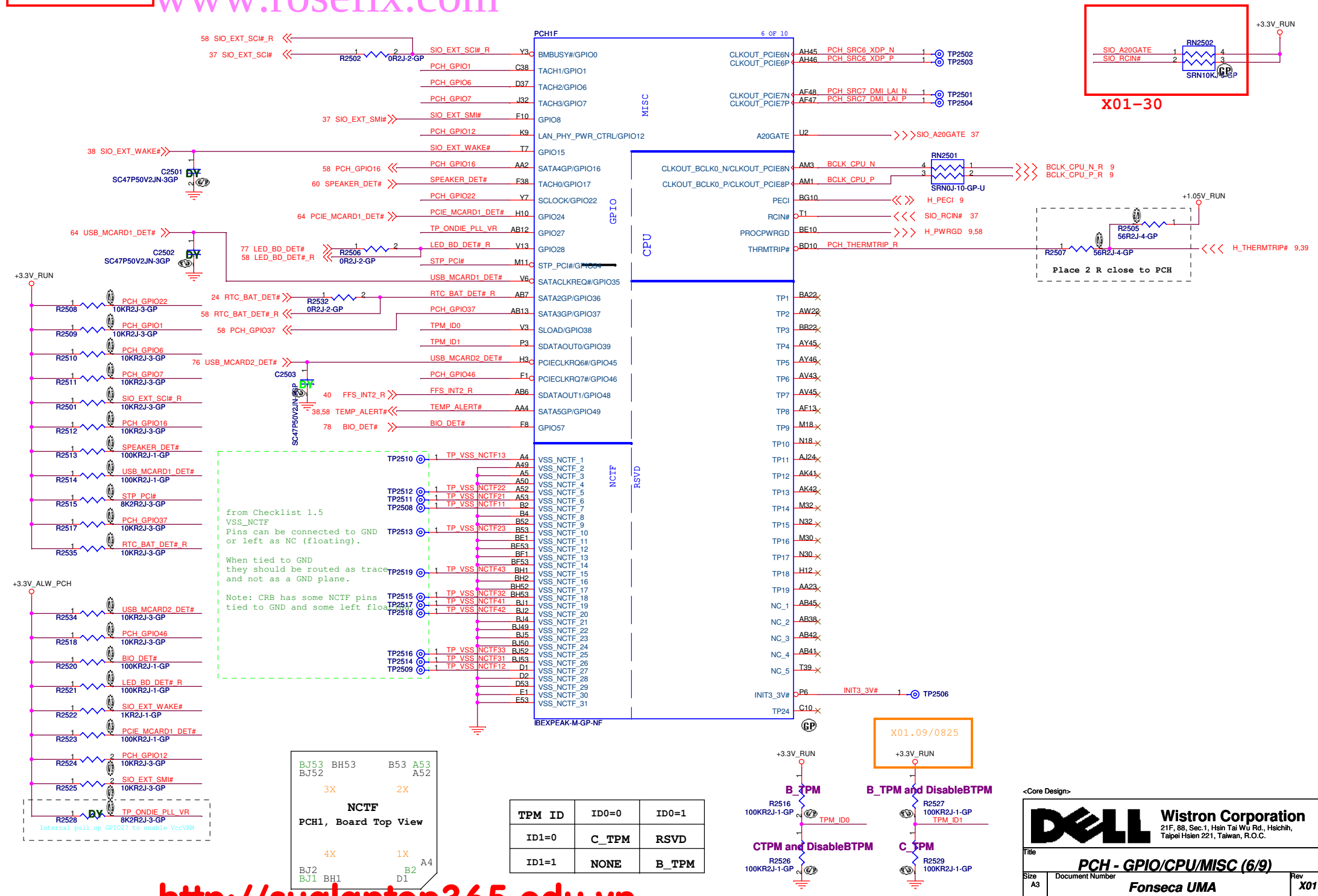

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<core_design>

Title: PCH - GPIO/CPU/MISC (6/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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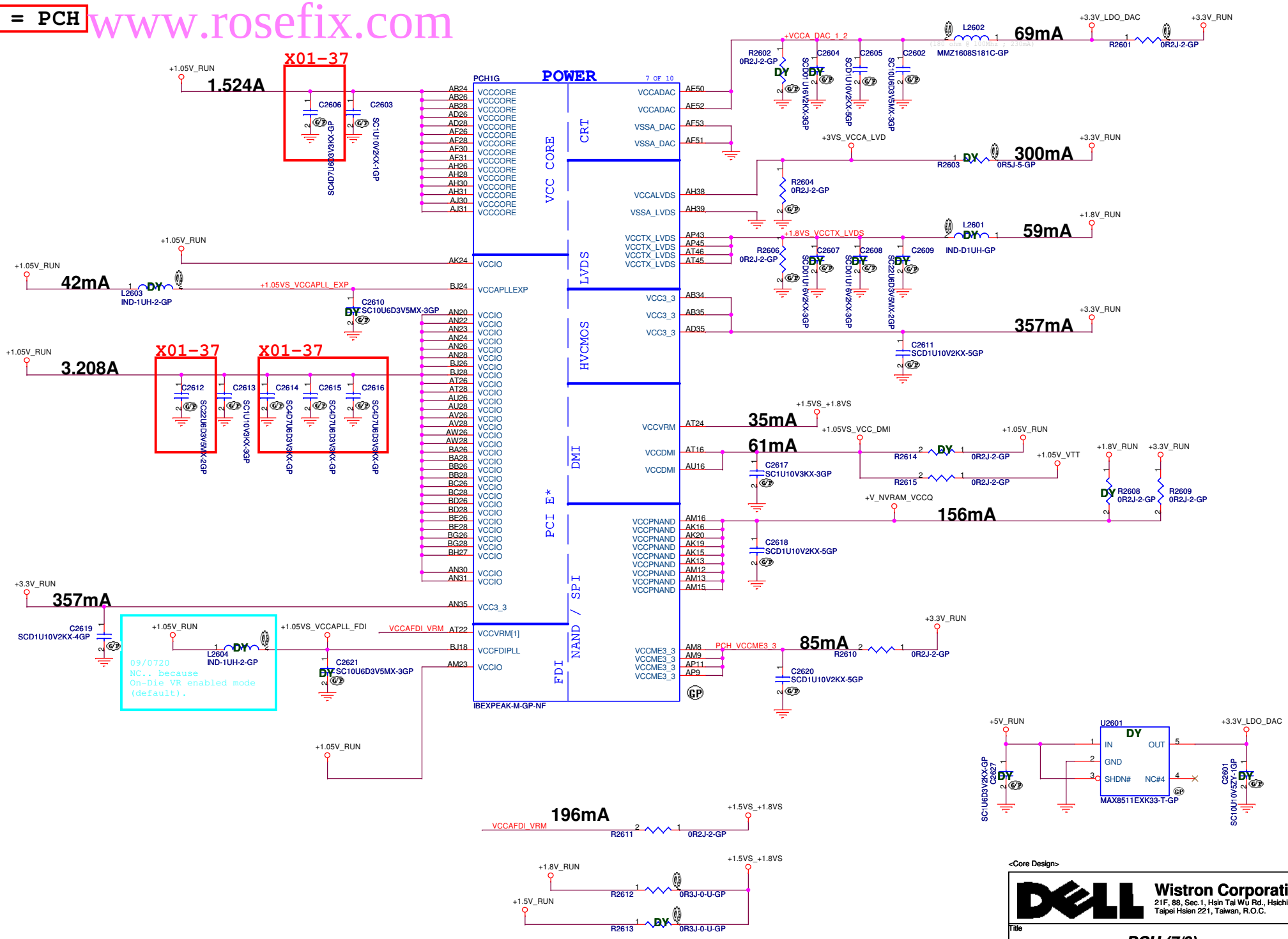
SSID = PCH

www.rosefix.com



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<Core Design>

Wistron Corporation
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Title: PCH (7/9)

Size	Document Number	Rev
A3	Fonseca UMA	X01

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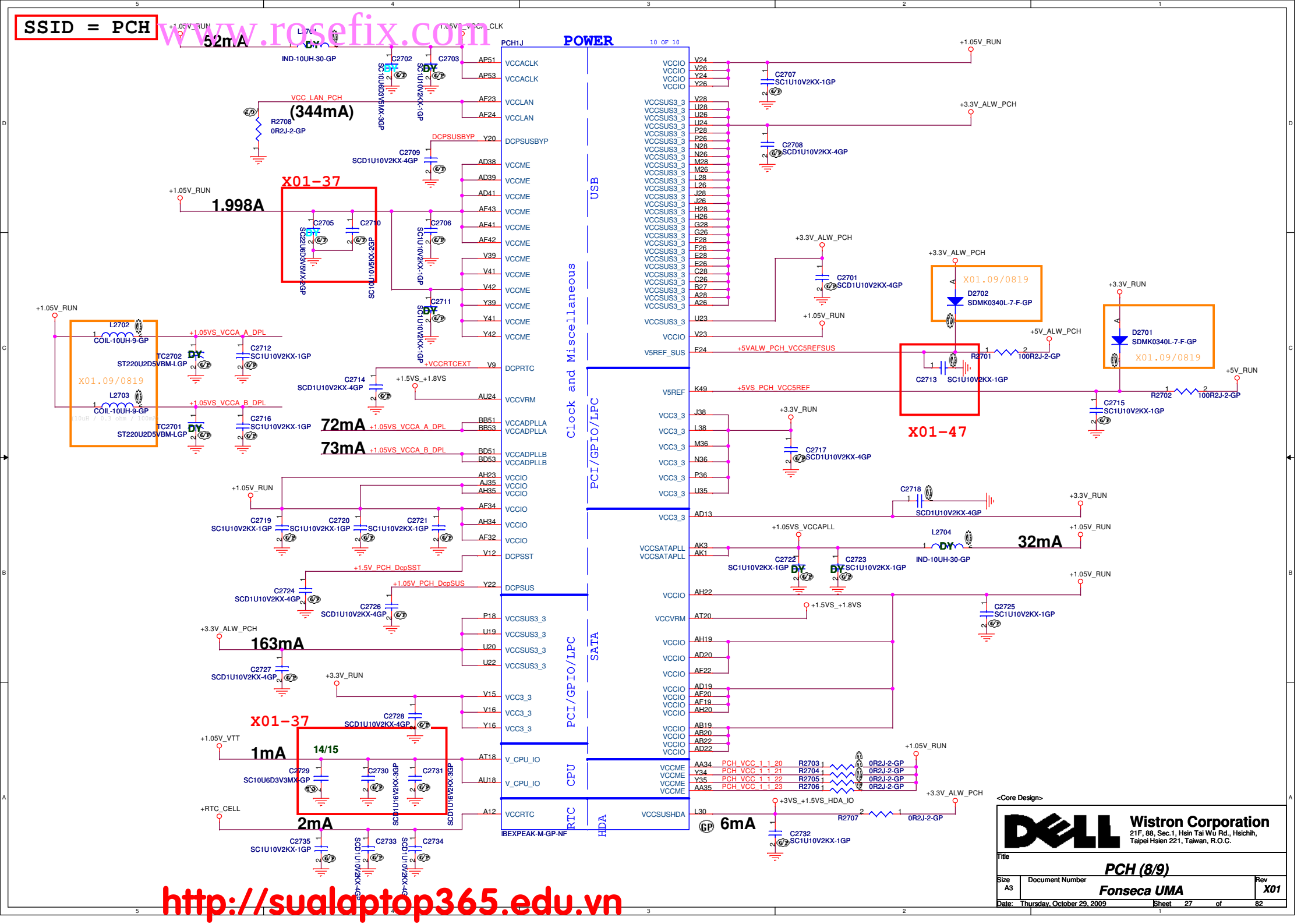
SSID = PCH
www.rosefix.com
POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
52mA
(344mA)
1.998A
X01-37
72mA
73mA
163mA
1mA
2mA
6mA
32mA
X01-47
X01.09/0819
14/15
+1.05V_RUN
+3.3V_ALW_PCH
+3.3V_RUN
+5V_ALW_PCH
+5V_RUN
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+1.05VS_VCCAPLL
+1.5VS_+1.8VS
+3VS_+1.5VS_HDA_IO
+1.05V_VTT
+RTC_CELL
+VCCRTCEXT
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+1.5V_PCH_DcpSST
+1.05V_PCH_DcpSUS
VCC_LAN_PCH
DCPSUSBYP
IND-10UH-30-GP
COIL-10UH-9-GP
ST220U2D5VBM-LGP
SDMK0340L-7-F-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
Fonseca UMA
Rev X01
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http://sualaptop365.edu.vn

SSID = PCH

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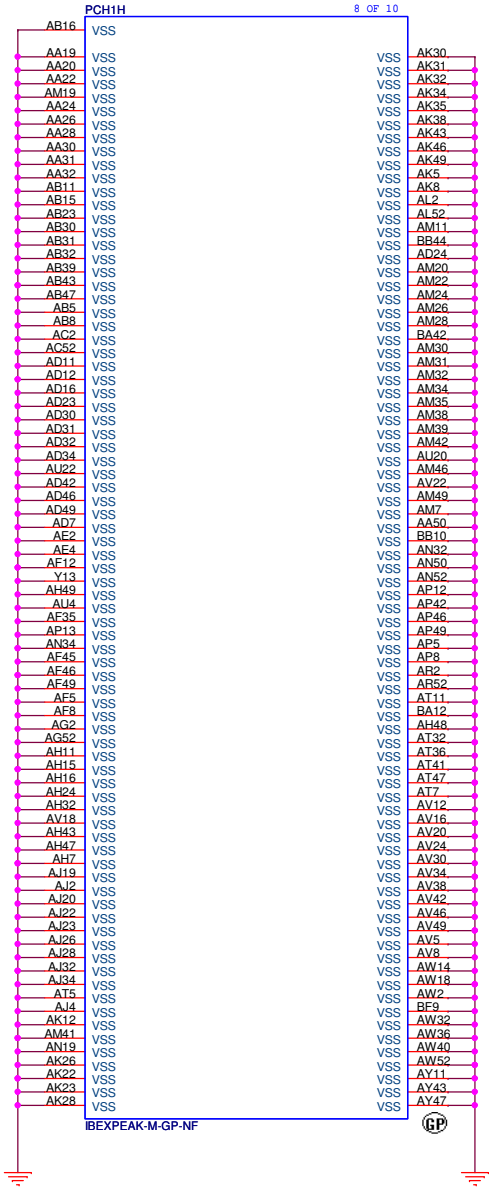

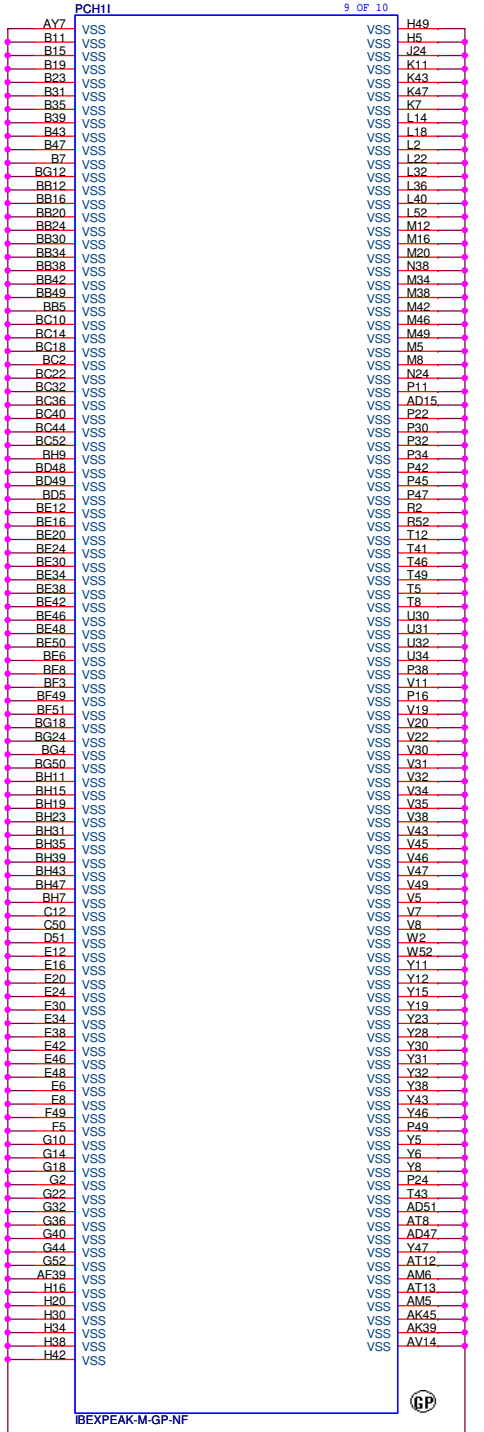

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Title: PCH (9/9)

Size: A3 | Document Number: Fonseca UMA | Rev: X01

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<Core Design>

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Title: Reserve

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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SSID = AUDIO

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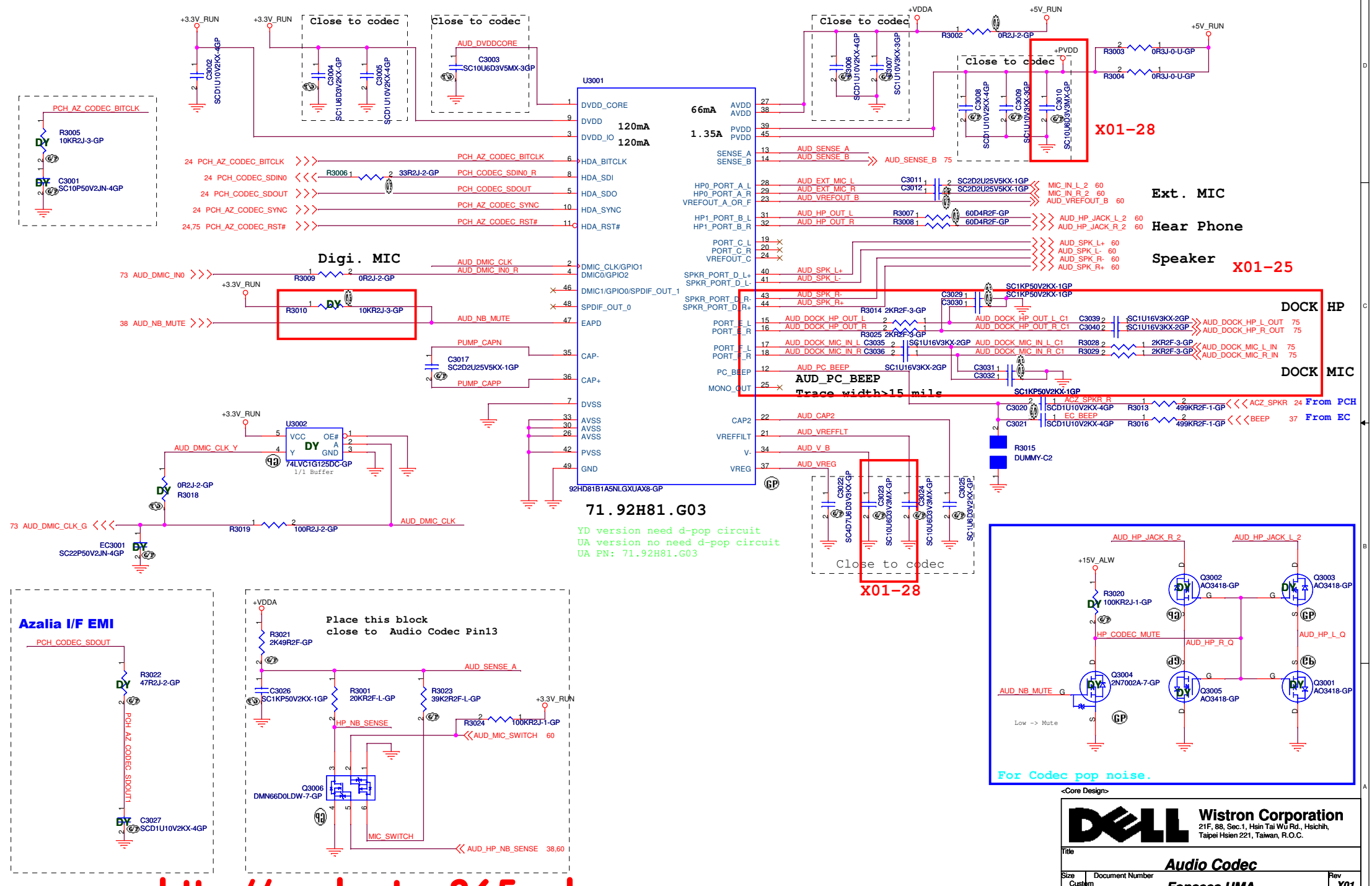

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<Core Design>

Wistron Corporation
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Title: Reserve

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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SSID = 1394

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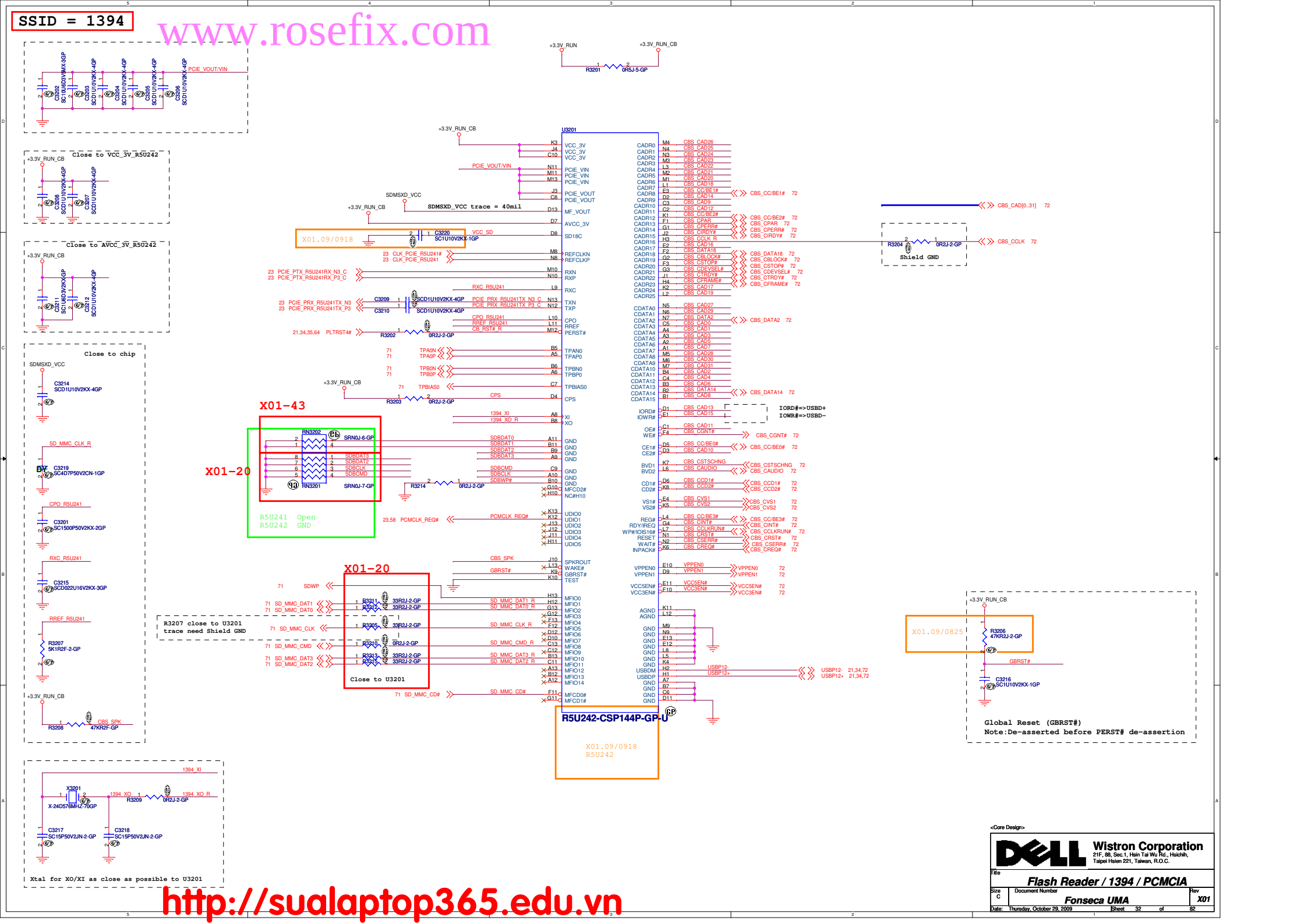

http://sualaptop365.edu.vn

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash Reader / 1394 / PCMCIA

Size: C | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 32 of 82

www.rosefix.com

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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SSID = SmartCard

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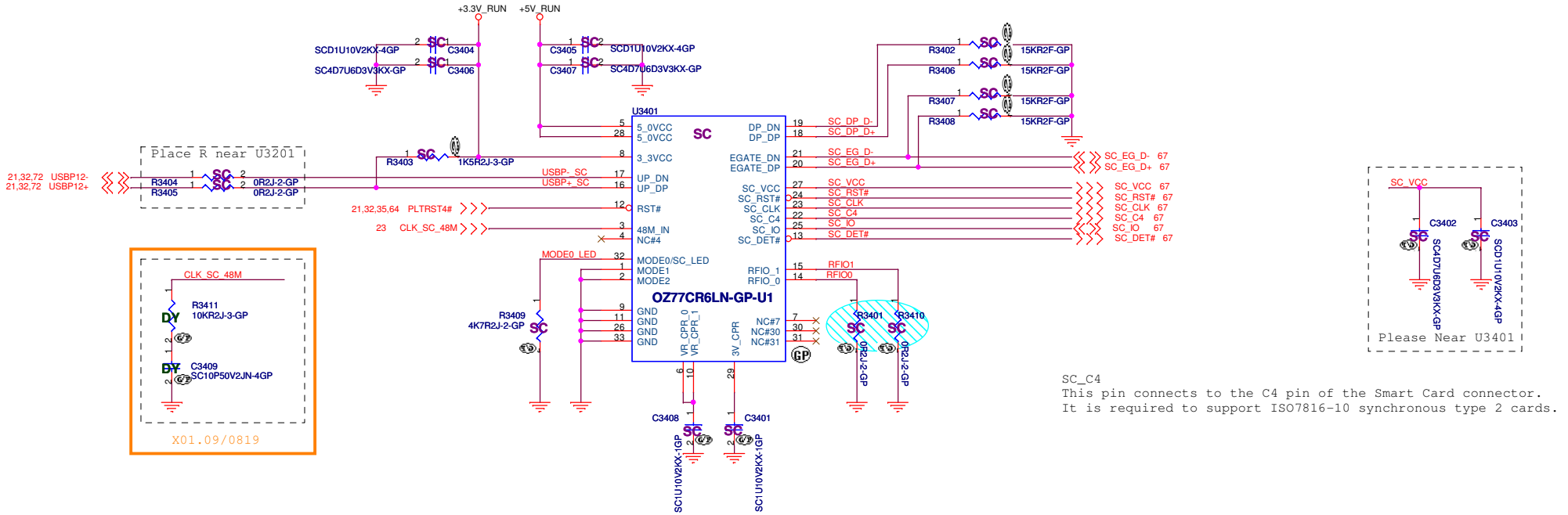
SmartCard Chip



SC_C4
This pin connects to the C4 pin of the Smart Card connector.
It is required to support ISO7816-10 synchronous type 2 cards.

VR filter.
An external capacitor shall connect to this terminal.

MODE0 / SC_LED	This terminal is an output indicating Smart Card activity; capable to drive an external LED device. The SC_LED terminal drives a low logic level during Smart Card data read/write activity, and is capable to source 12mA of IOL current to drive an external LED circuit. When RST# is asserted, this terminal is sampled to select the downstream port configuration for DP_DP and DP_DN (Internal Port 1). When sampled low (4.7k), the downstream port device is removable. When sampled high, the downstream port is a non-removable device. Includes internal input pull-up resistor.
MODE1	Test Pin. This terminal shall be externally connected to GND.
MODE2	Test Pin. This terminal shall be externally connected to GND.

RFIO_0 RFIO_1	Contactless Smart Card Interface Signal 0 and 1. This signal provides detection and data communication with an external RF device. If contactless is disabled, then this terminal shall be pulled-down to GND through a pull-down resistor, or directly connected to GND.

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Smart Card (OZ77CR6LN)
Size: Custom | Document Number: Fonseca UMA | Rev: X01
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SSID = LOM

Symbol : 71.05761.00U

Product : P802H (Rev:B0)

www.rosefix.com

X01.09/0825

LOM_SMBCLK

LOM_SMBDAT

U3503

DMN66D0LDW-7-GP

LAN_SMBCLK 37

LAN_SMBDAT 37

Core Power Decoupling

VDDIOPower Decoupling

Put 0.1u cap close to Chip

Co-Layout

U3505

U3506

X01-22

U3507

M25PE80-VMN6TP-GP

U3505

AT45DB081D-SSU-GP

72.45081.B01

U3506

AT45DB081D-SU-SL955-GP

72.45081.C01

8Mb for 5761E:

Main source: 72.45081.C01(Big PAD)

2nd source: 72.45081.B01(Small PAD)

Populate resister for debug

U3501A

1 OF 2

BCM5761EA0KFBG-GP

U3501B

2 OF 2

BCM5761EA0KFBG-GP

DOCKED

SEL 0:RJ45.

SEL 1:Dock.

X01.09/0917

CTPM and DisableBTPM

X01.09/0819

Reserve for EMI

Close to the power pins and

0.1u cap should be closer to Chip

X01.09/0918

Place crystal less

than 0.75" (~1.9cm)

from LAN Controller

Logic High Voltage must

be 0.7V to 2.75V

Design current: 89.6mA

Max current: 128mA

X01-39

Design Current: 627mA

<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.

Title: GLAN - BCM5761E

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 35 of 82

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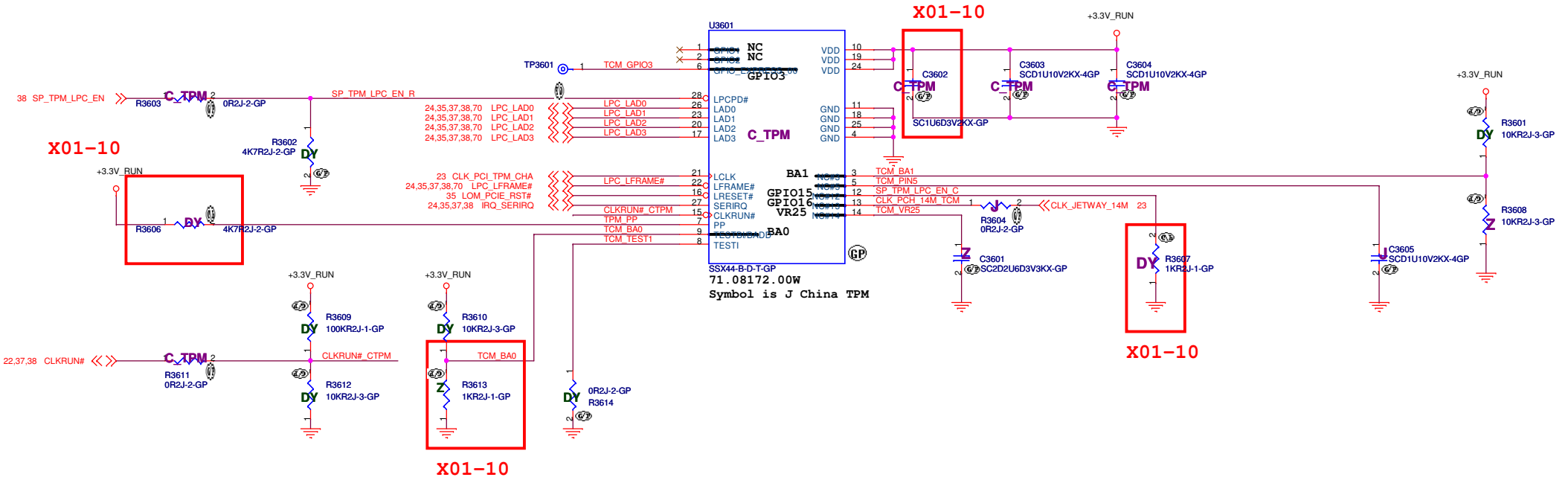
SSID = TCM

www.rosefix.com

Symbol : Jetway, but linked to ZTE
Product : 71.08172.00W (ZTE)

China TPM Chip



Z

Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

Default EE/EF as Amy recommended

J

	1(default)	0
PIN12	FLASH	SRAM

J has internal PU with PIN12.

<Core Design>

Wistron Corporation
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Title: TCM
Size: Custom | Document Number: Fonseca UMA | Rev: X01
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SSID = KBC

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MEC5045-LZY-GP

U3701

PS/2 INTERFACE
GPIO007/I2C1D_DATA/PS2_CLK0B/I2C3A_DATA
GPIO010/I2C1D_CLK/PS2_DAT0B/I2C3A_CLK
GPIO110/PS2_CLK2/GPTP-IN6
GPIO111/PS2_DAT2/GPTP-OUT6
GPIO112/PS2_CLK1A
GPIO113/PS2_DAT1A
GPIO114/PS2_CLK0A
GPIO115/PS2_DAT0A
GPIO154/I2C1C_DATA/PS2_CLK1B
GPIO155/I2C1C_CLK/PS2_DAT1B

JTAG INTERFACE
GPIO145/JTAG_TDI
GPIO146/I2C1K_CLK/JTAG_TDO
GPIO147/I2C1J_DATA/I2C2C_DATA/JTAG_CLK
GPIO150/I2C1J_CLK/I2C2C_CLK/JTAG_TMS
JTAG_RST#

0 = Reset JTAG I/F
1 = Disable

FAN PWM & TACH
GPIO050/FAN_TACH1
GPIO051/FAN_TACH2
GPIO052/FAN_TACH3
GPIO053/PWM0
GPIO054/PWM1
GPIO055/PWM2
GPIO056/PWM3

BC-LINK
GPIO123/BCM_A_CLK
GPIO122/BCM_A_DAT
GPIO121/BCM_A_INT#
GPIO022/BCM_B_CLK
GPIO023/BCM_B_DAT
GPIO024/BCM_B_INT#
GPIO044/BCM_C_CLK
GPIO043/BCM_C_DAT
GPIO042/BCM_C_INT#
GPIO047/LSBCM_D_CLK
GPIO046/LSBCM_D_DAT
GPIO045/LSBCM_D_INT#
GPIO032/GPTP-IN3/BCM_E_CLK
GPIO031/GPTP-OUT2/BCM_E_DAT
GPIO30/GPTP-IN2/BCM_E_INT#

HOST INTERFACE
GPIO011/SMI#
GPIO061/LPCPD#
LDRQ#
SER_IRQ
LRESET#
PCI_CLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLKRUN#
GPIO100/EC_SCI#

MASTER CLOCK
XTAL1
XTAL2
GPIO160/32KHZ_OUT

MISC INTERFACE
GPIO021/RC_ID1
GPIO020/RC_ID2
GPIO025/UART_CLK
GPIO120/UART_TX
GPIO124/GPTP-OUT5/UART_RX
VCC_PRWGD
GPIO060/KBRST
GPIO101/ECGP_SCLK
GPIO103/ECGP_SIN
GPIO105/ECGP_SOUT
GPIO102/HSPI_SCLK
GPIO104/HSPI_MISO
GPIO106/HSPI_MOSI
GPIO116/MSDATA
GPIO117/MSCLK
GPIO127/A20M
GPIO153/LED3
GPIO156/LED1
GPIO157/LED2
FWP#

GENERAL PURPOSE I/O
GPIO001/ECSPI_CS1
GPIO002/ECSPI_CS2
GPIO014/GPTP-IN7/HSPI_CS1
GPIO040/GPTP-OUT3/HSPI_CS2
GPIO015/GPTP-OUT7
GPIO016/GPTP-IN8
GPIO017/GPTP-OUT8
GPIO26/GPTP-IN1
GPIO27/GPTP-OUT1
GPIO041
GPIO107/nRESET_OUT
GPIO125/GPTP-IN5
GPIO126
GPIO151/GPTP-IN4
GPIO152/GPTP-OUT4

SMBUS INTERFACE
GPIO003/I2C1A_DATA
GPIO004/I2C1A_CLK
GPIO005/I2C1B_DATA
GPIO006/I2C1B_CLK
GPIO012/I2C1H_DATA/I2C2D_DATA
GPIO013/I2C1H_CLK/I2C2D_CLK
GPIO130/I2C2A_DATA
GPIO131/I2C2A_CLK
GPIO132/I2C1G_DATA
GPIO140/I2C1G_CLK
GPIO141/I2C1F_DATA/I2C2B_DATA
GPIO142/I2C1F_CLK/I2C2B_CLK
GPIO143/I2C1E_DATA
GPIO144/I2C1E_CLK

DELL PWR SW INF
BGPO0
VCI_IN2#
VCI_OUT
VCI_IN1#
VCI_IN0#
VCI_OVRD_IN
VCI_IN3#

X01-12

X01-14

X01-19

X3701 X-32D768KHZ-40GPU

Place close to Pin58

Fonseca UMA Revision

SYSTEM_ID	BOARD_ID Cap. Value	BOARD_ID Cap. Value	REV
	4700pF	240k ohm	X00
2k ohm	4700pF	130k ohm	X01
4700pF	4700pF	62k ohm	X02
	4700pF	33k ohm	-1

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC - MEC5045
Size: Custom
Document Number: Fonseca UMA
Rev: X01
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SSID = KBC

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X01.09/0917

X01.09/0918

X01-30

ECE5028-LZY-GP

U3801

VGA_IDENTIFY
High = Discrete
Low = UMA

Place close to Pin.A28

Place close to Pin.A32

CRD_DET1	CRD_DET0	Function
Low	Low	No Option Installed
Low	High	Smartcard
High	Low	Cardbus
High	High	Express Card

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIO - MEC5028

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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SSID = Thermal

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EMC4022 SMBus Addr = {5E} / {5F}

BC Bus clock and data signal trace length should be matched with +/- 0.1 inch.

37 BC_DAT_EMC4022

37 BC_CLK_EMC4022

X01-21 X01-21

X01-45

Q3902 and C3902 Place under CPU

C3902 SC100P50V2JN-3GP

Q3902 MMBT3904-7-F-GP

C3901 SC470P50V2KX-3GP close to the Guardian pins

Place C3902 as close to the Q3902 as possible

REM_DIODE4_N, REM_DIODE4_P routing together.
Trace width / Spacing = 10 / 10 mil
Place near the bottom SODIMM

Q3905 and C3906 Place near DIMM

C3906 SC100P50V2JN-3GP

Q3905 MMBT3904-7-F-GP

Place C3906 as close to the Q3903 as possible

Skin Temp Sensor

C3904 SC100P50V2JN-3GP

Q3901 MMBT3904-7-F-GP

Place optimally between CPU and MEM

Place C3904 as close to the Q3901 as possible

C3905 SC2200P50V2KX-2GP close to the Guardian pins

Q3903 and C3903 Place near WLAN

C3903 SC100P50V2JN-3GP

Q3903 MMBT3904-7-F-GP

Place C3903 close to the Q3903 as possible

C3908 SC2200P50V2KX-2GP close to the Guardian pins

U3901

EMC4022-1-EZK-TR-1-GP-U

SMDATA/BC_DATA
SMCLK/BC_CLK
REM_DIODE1_P
REM_DIODE1_N
DP1/VREF_T
DN1/THERM
REM_DIODE4_P
REM_DIODE4_N
DP2/DN4
DN2/DP4
REM_DIODE3_P
REM_DIODE3_N
DP3/DN5
DN3/DP5
VIN
VCP
SYS_IMON_4022
CPU_IMON_4022
3VSUS_THRM
VDD
RTC_PWR3V
ATF_INT#/BC_IRQ#
POWER_SW#
ACAVAIL_CLR
GPIO3/PWM/THERMTRIP_SIO
SYS_SHDN#
VDD_PWRGD
3V_PWROK#
THERMTRIP2#
THERMTRIP3#
VSET
ADDR_MODE/XEN
VDD_HA
VDD_HB
VDD_L
FAN_OUTA
FAN_OUTB
TACH/GPIO1
GPIO2
TEST1
TEST2
GND_SLG

BC_INT#_EMC4022
POWER_SW_IN#_4022
ACAV_IN
THERMTRIP_SIO
THERM_STP#

SYS_IMON
R3902 12K7R2F-GP
R3903 5K62R2F-GP
PC3901 SCD22U25V3KX-GP
Place together Near U3901

R3917
if use 4.7k-J, 2.1% inaccuracy for IMON
if use 1k-J, 0.5% inaccuracy for IMON
if use 470-J, 0.3% inaccuracy for IMON
Place near fork into U3901
R3917 1KR2F-3-GP CPU_IMON 12,47

R3907 10KR2J-3-GP +3.3V_ALW
BC_INT#_EMC4022 37
R3909 10KR2J-3-GP ACAV_IN 37,45
+3.3V_SUS
THERM_STP# 46
R3912 47KR2J-2-GP +RTC_CELL

+3.3V_SUS
R3906 22R2J-2-GP
C3918 SC1U6D3V2KX-GP
C3909 SCD1U10V2KX-4GP
+RTC_CELL
C3910 SC1U6D3V2KX-GP
R3910 8K2R2J-3-GP
R3911 100KR2J-1-GP
R3901 1KR2J-1-GP
THERM_VDD_PWRGD
THERM_3V_PWROK#
PCH_PWRGD#
+1.05V_RUN
R3913 2K2R2J-2-GP
THERM_B1
Q3906 MMBT3904-7-F-GP
9,25 H_THERMTRIP#
C3911 SCD1U10V2KX-4GP

Rset=953, Tp=88degree

C3912 SCD1U10V2KX-4GP
R3915 953R2F-GP
3VSUS_THRM_1
R3914 4K7R2J-2-GP
THERMAL_VSET

X01.09/0825
Update to 4022 Rev.B

R3916 8K2R2J-3-GP
C3913 SCD1U10V2KX-4GP

58 FAN1_VOUT
FAN1_VOUT
58 FAN1_TACH_FB
FAN1_TACH_FB
FAN1_DET#
FAN1_DET# 58

+5V_RUN
C3914 SC10U10V5KX-2GP
C3915 SCD1U10V2KX-4GP
+3.3V_RUN
R3927 100KR2J-1-GP

DOCK_PWR_SW#_R
R3918 0R2J-2-GP
DOCK_PWR_SW# 37
D3901 BAT54A-3
POWER_SW_IN#_R
R3921 0R2J-2-GP
POWER_SW_IN# 37
+RTC_CELL
R3920 100KR2J-1-GP
POWER_SW_IN#_4022
R3924 0R2J-2-GP
R3925 0R2J-2-GP

+3.3V_SUS
R3922 100KR2J-1-GP
PCH_PWRGD#
Q3908 2N7002A-7-GP
38,47 IMVP_PWRGD
R3926 0R2J-2-GP IMVP_PWRGD_R

+3.3V_RUN
C3916 SC10U10V5KX-2GP
C3917 SCD1U10V2KX-4GP

http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal, Fan controller

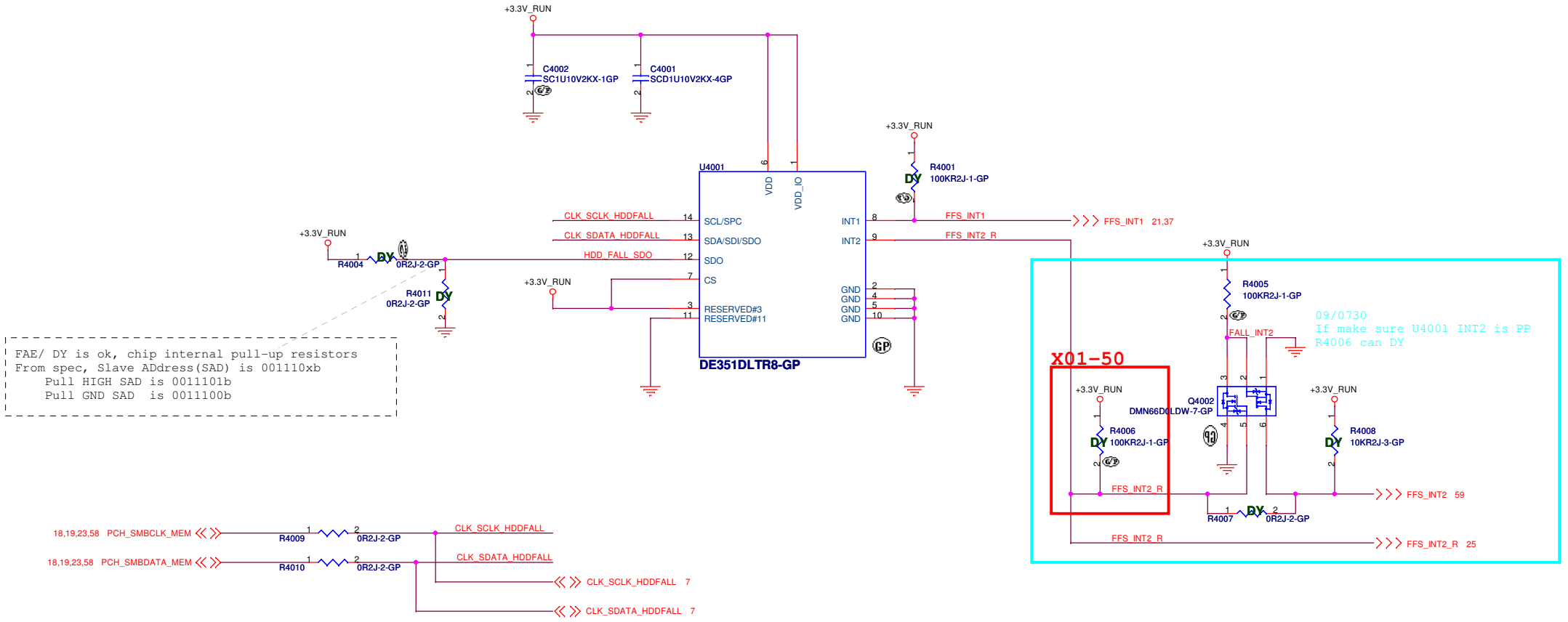
Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 39 of 82

SSID = User.Interface

www.fosefix.com

Free Fall Sensor



Layout Note
- no via, trace, under the sensor
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor
Size: A3 | Document Number: Fonseca UMA | Rev: X01
Date: Thursday, October 29, 2009 | Sheet 40 of 82

http://sualaptop365.edu.vn

SSID = Reset.Suspend

www.rosefix.com

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power On Logic

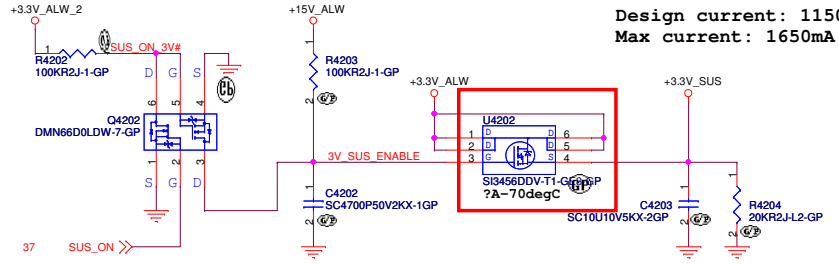
Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 41 of 82

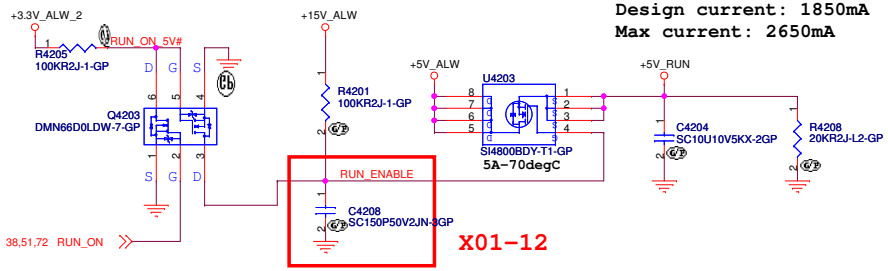
http://sualaptop365.edu.vn

SSID = Reset Suspend

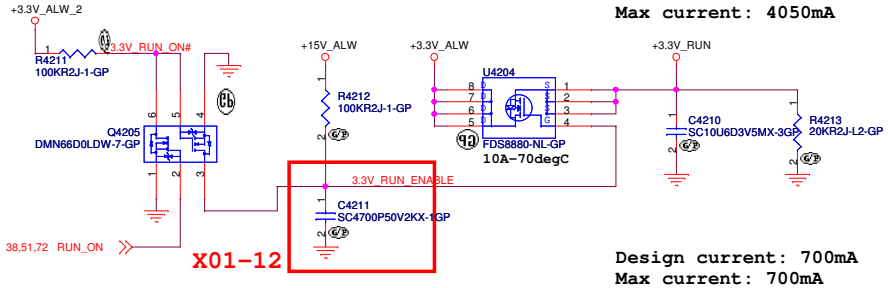
www.rosefix.com



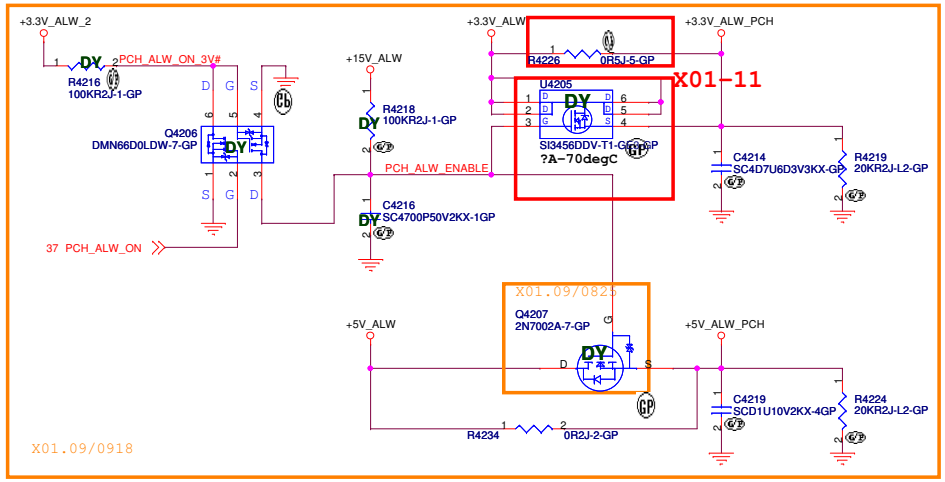
Design current: 1150mA
Max current: 1650mA



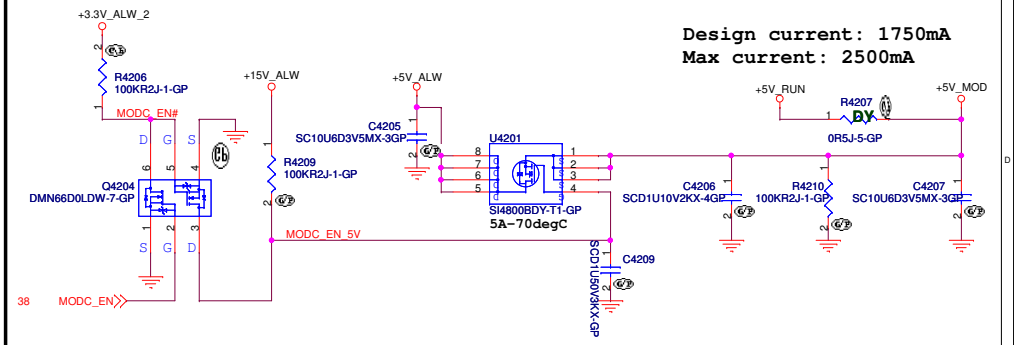
Design current: 1850mA
Max current: 2650mA



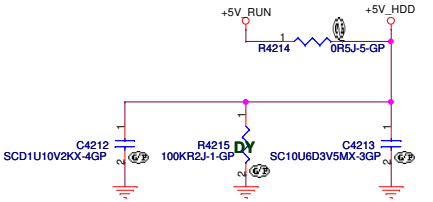
Design current: 2850mA
Max current: 4050mA



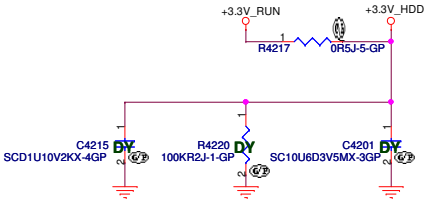
Design current: 700mA
Max current: 700mA

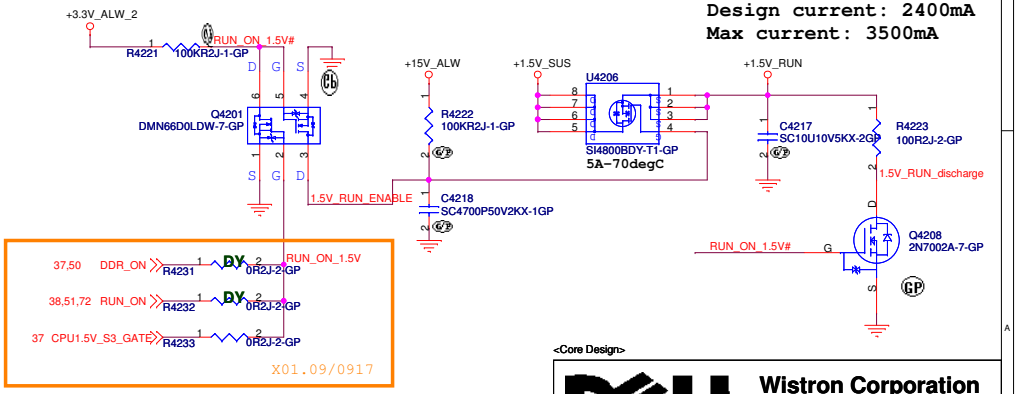


Design current: 1750mA
Max current: 2500mA



Design current: 700mA
Max current: 1000mA





Design current: 2400mA
Max current: 3500mA

http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 42 of 82

SSID = PWR.Support

www.rosefix.com

Adapter In

DC IN CONN	
PIN 2,3	DC_IN+
PIN 4,5	DC_IN-
PIN 1	ID
PIN 6,7,8,9	GND

PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

TABLE
MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R411	8.45K 1%	DUMMY	DUMMY
C98	0.01uF	0.1uF	0.1uF
C459	0.1uF 10V	DUMMY	200P 10V
C5	1uF 10V	DUMMY	1uF 10V
R16	365K 1%	215K 1%	309K 1%
R434	0 5%	10 5%	0 5%
R414	0 5%	10 5%	0 5%
C473	DUMMY	0.22uF	0.1uF
C457	DUMMY	0.22uF	0.1uF
C442	0.01uF	DUMMY	DUMMY
C453	0.1uF 10V	DUMMY	DUMMY
C36	220pF 50V	DUMMY	DUMMY
D23	RB751V-40	DUMMY	RB751V-40
C58	3.3nF	DUMMY	DUMMY
R64	1 1%	0 5%	0 5%
R394	100 5%	0 5%	0 5%
R110	0 5%	8.45K 1%	8.45K 1%
R401	10K 5%	2.2K 5%	4.7K 5%
C441	0.01uF	0.01uF	DUMMY
C449	0.01uF	0.01uF	DUMMY
R397	1K 5%	DUMMY	DUMMY
Q41	ISS355	DUMMY	DUMMY
C16	1uF 10V	1uF 10V	DUMMY
R30	33 1%	33 1%	DUMMY
R408	DUMMY	DUMMY	0 5%
R400	DUMMY	DUMMY	200K 5%
R403	DUMMY	DUMMY	7.5K 5%
C450	DUMMY	DUMMY	51P 10V
C444	DUMMY	DUMMY	2000P 10V
C448	DUMMY	DUMMY	130P 10V
C446	DUMMY	DUMMY	0.1uF
C483	DUMMY	DUMMY	0.1uF
R438	10K 1%	10K 1%	DUMMY
R412	DUMMY	DUMMY	10k 5%
R440	15.8K 1%	15.8K 1%	DUMMY
R407	DUMMY	10K 5%	DUMMY
R9	0 5%	10 5%	0 5%
C482	DUMMY	DUMMY	DUMMY
C12	DUMMY	DUMMY	DUMMY
R435	0 5%	10 5%	0 5%

MAX 8731A/ISL88731

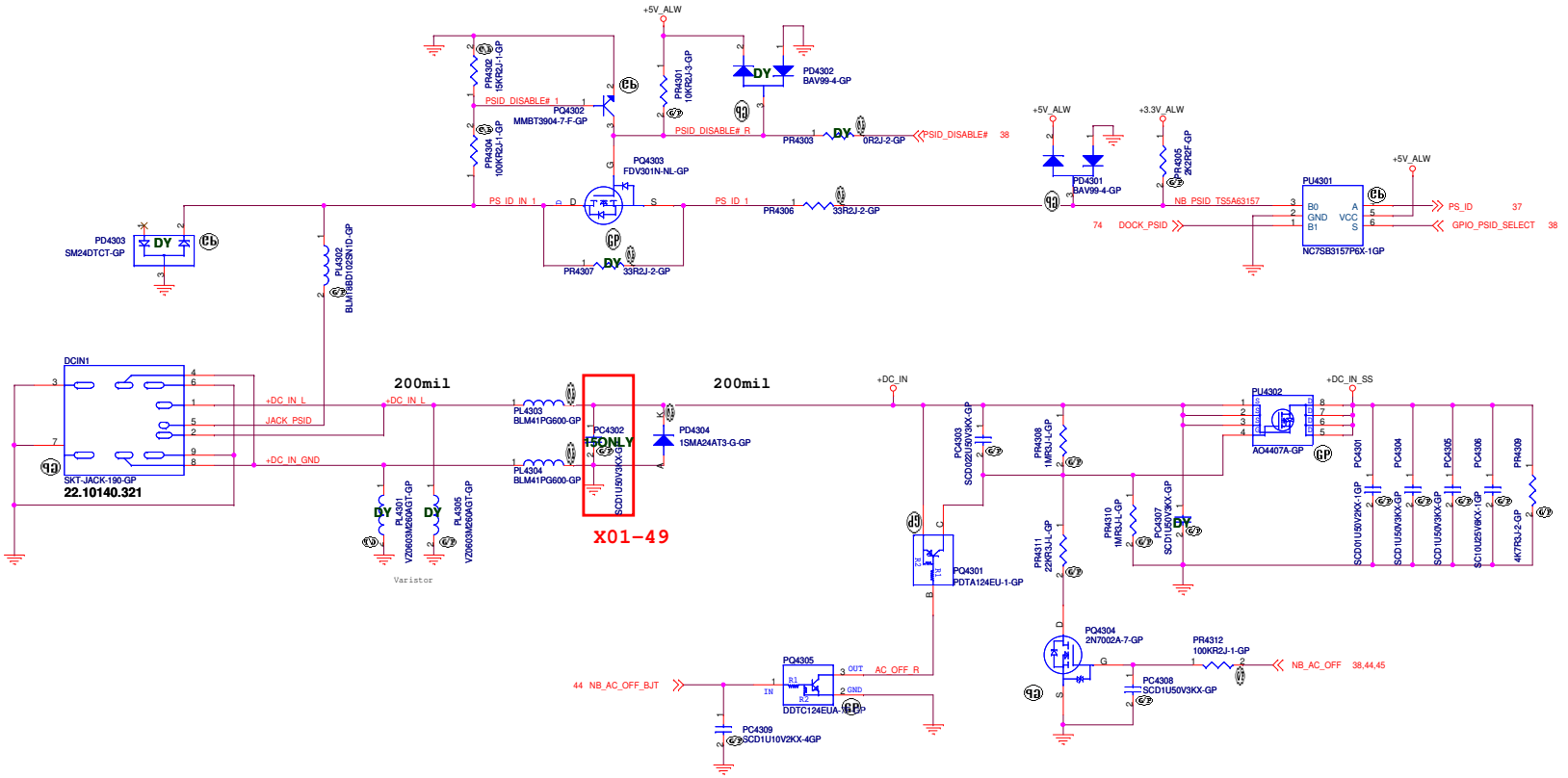
Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

*R504 is populated if ADAPT_TRIP_SEL is used
to program for the next lower adapter.

BQ247451

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

*R504 is populated if ADAPT_TRIP_SEL is used
to program for the next lower adapter.



http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC IN Jack
Size: C
Document Number: Fonseca UMA
Rev: X01
Date: Thursday, October 29, 2009
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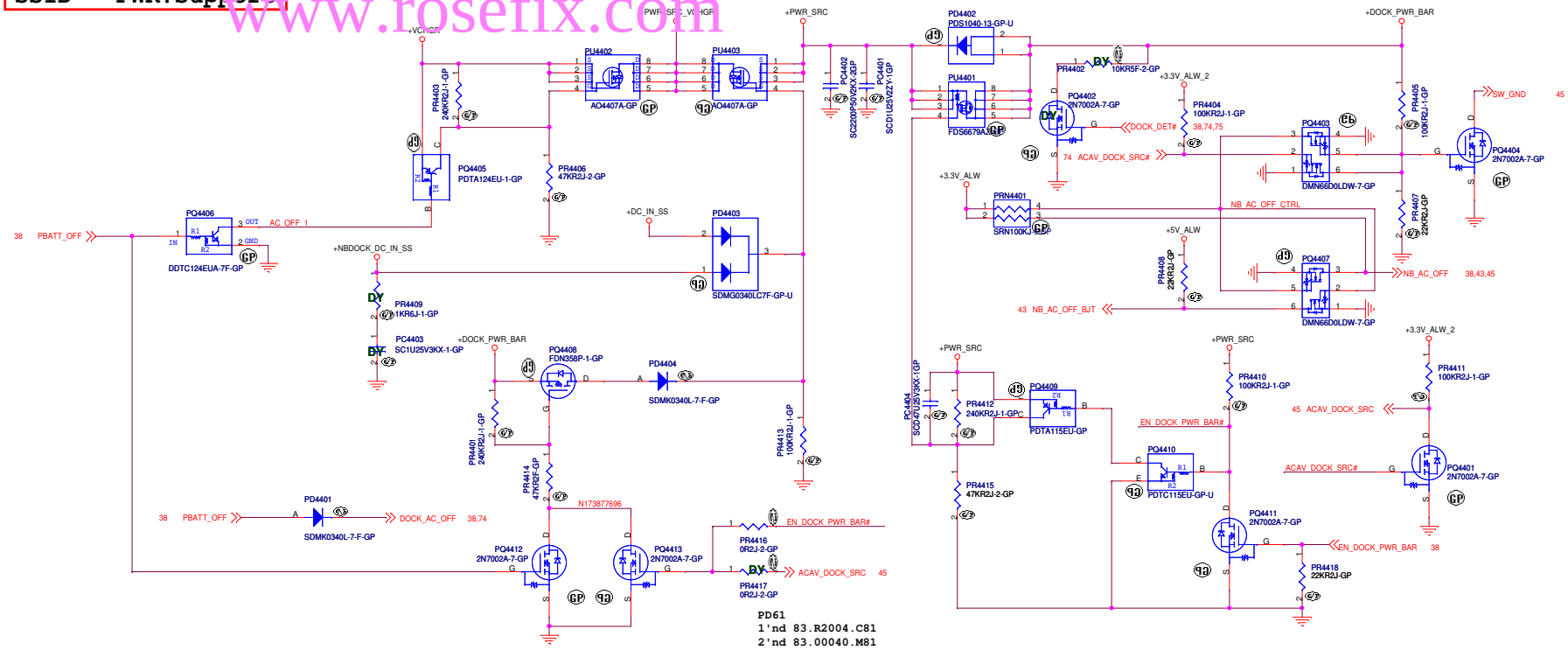
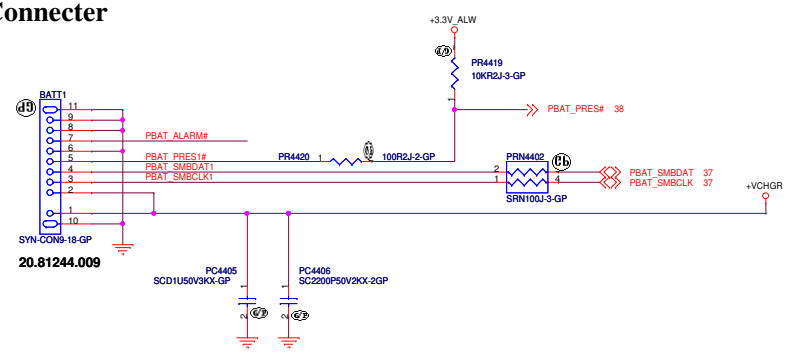
www.rosefix.com

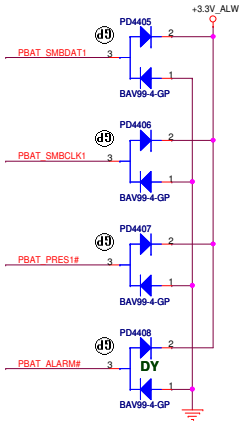
SSID = PWR.Support



SSID = RBATT

Batt Connecter





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DOCK DCIN/BATT Connector

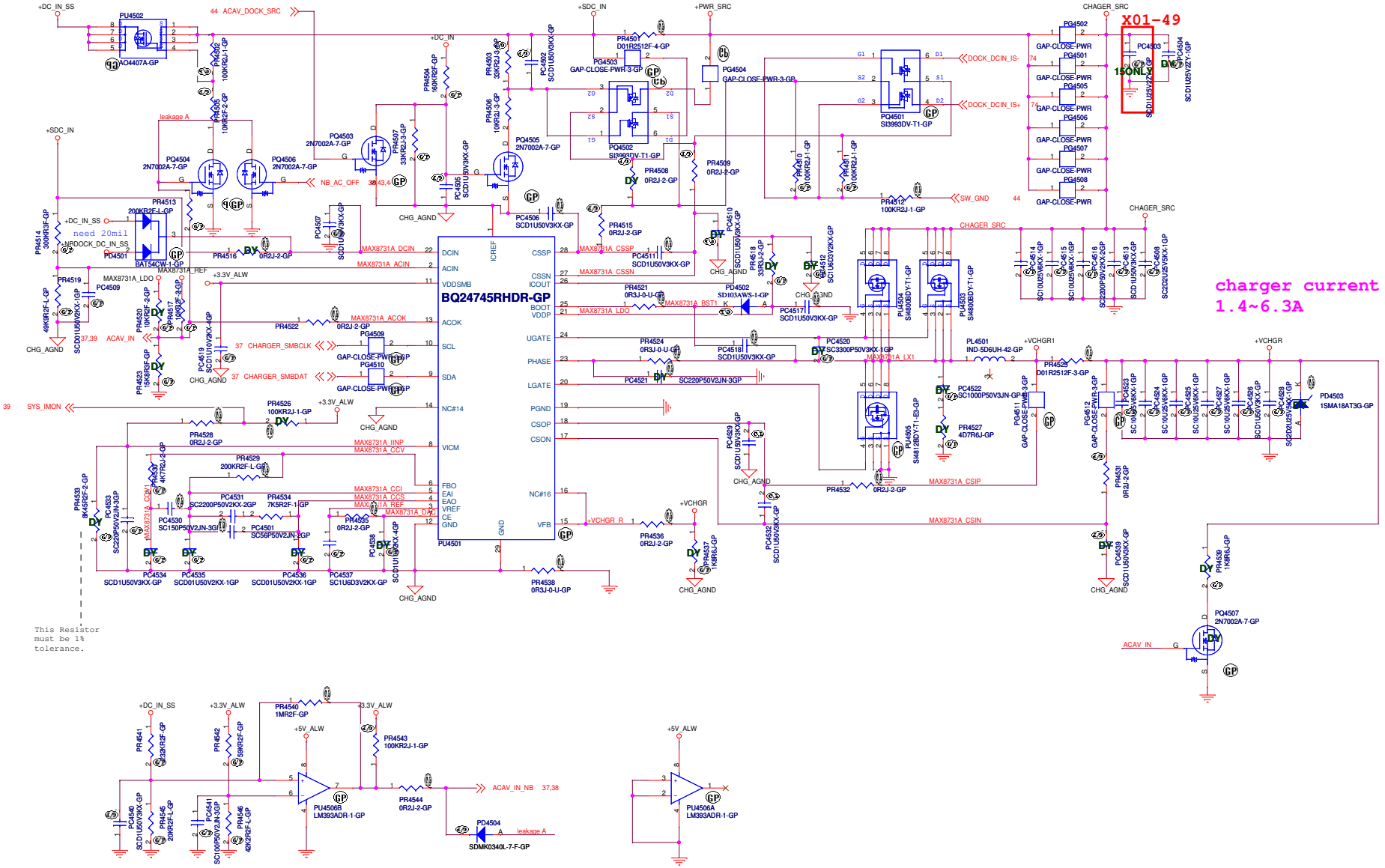
Size	Document Number	Rev
C	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 44 of 82

http://sualaptop365.edu.vn

SSID = Charger

www.rosefix.com



http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

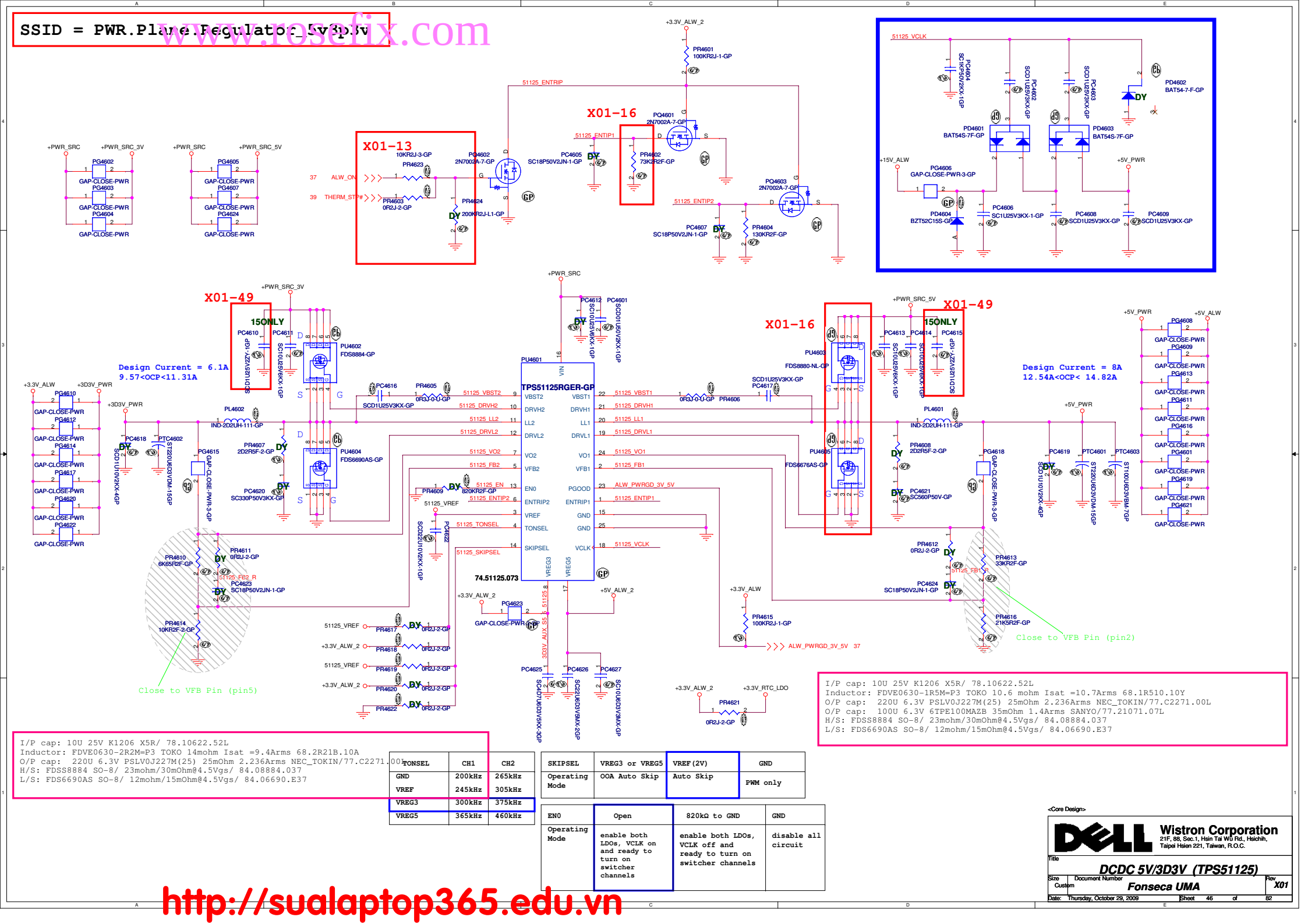
Title: Battery Charger

Size	Document Number	Rev
C	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 45 of 82

SSID = PWR.Plane.Regulator_5v3p3v

www.rosefix.com



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDVE0630-2R2M=P3 TOKO 14mohm Isat =9.4Arms 68.2R21B.10A
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDVE0630-1R5M=P3 TOKO 10.6 mohm Isat =10.7Arms 68.1R510.10Y
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V 6TPE100MAZB 35mOhm 1.4Arms SANYO/77.21071.07L
H/S: FDSS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

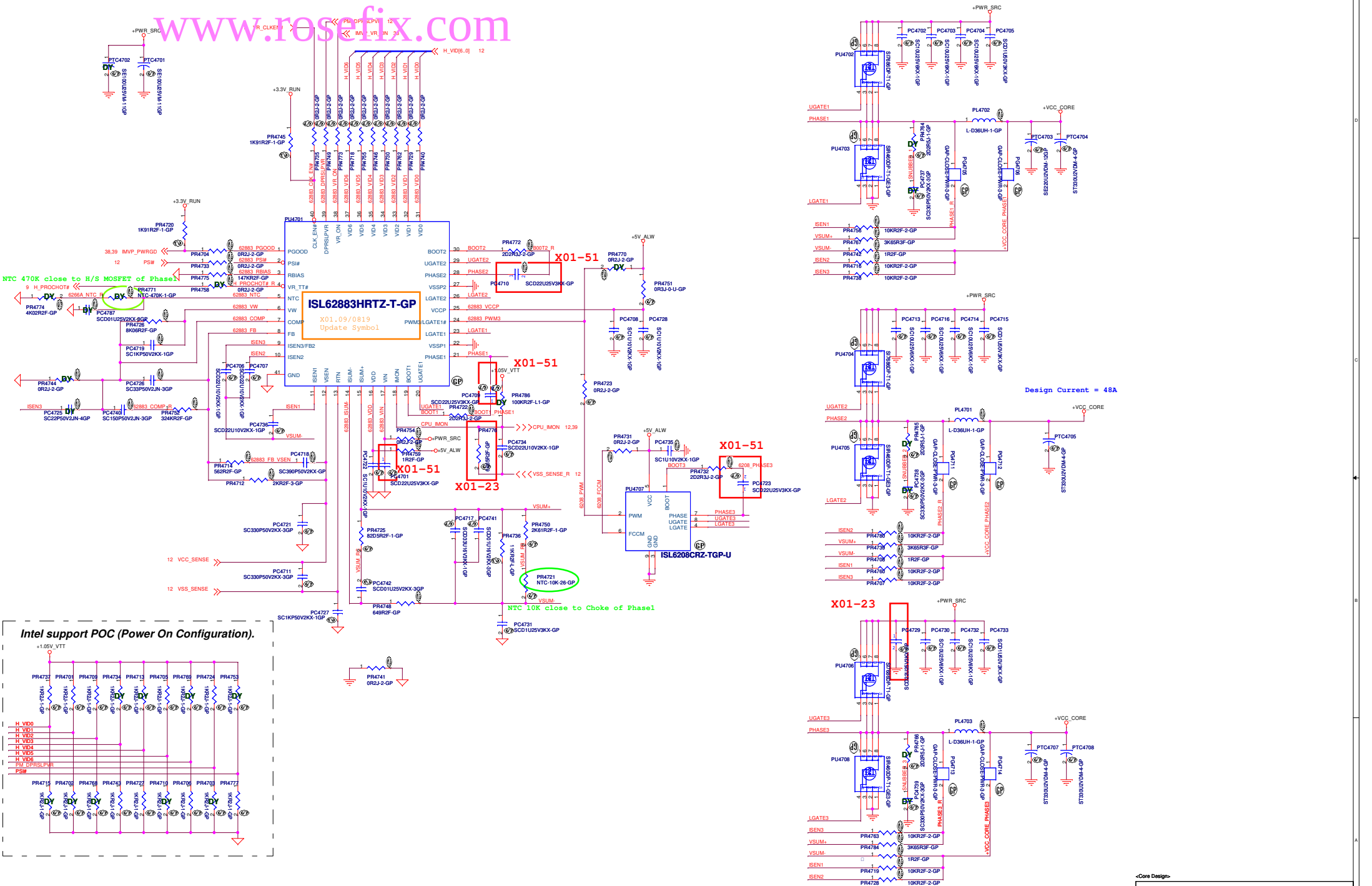
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)
Size: Custom | Document Number: Fonseca UMA | Rev: X01
Date: Thursday, October 29, 2009 | Sheet 46 of 82

http://sualaptop365.edu.vn

www.rosefix.com



http://sualaptop365.edu.vn

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE
Size: A2 | Document Number: Fonseca UMA | Rev: X01
Date: Friday, October 30, 2009 | Sheet 47 of 82

www.rosefix.com

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca UMA* | Rev: *X01*

Date: Thursday, October 29, 2009 | Sheet 48 of 82

http://sualaptop365.edu.vn

SSID = PWR.Plane.Regulator_1p05v

www.rosefix.com

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.05V

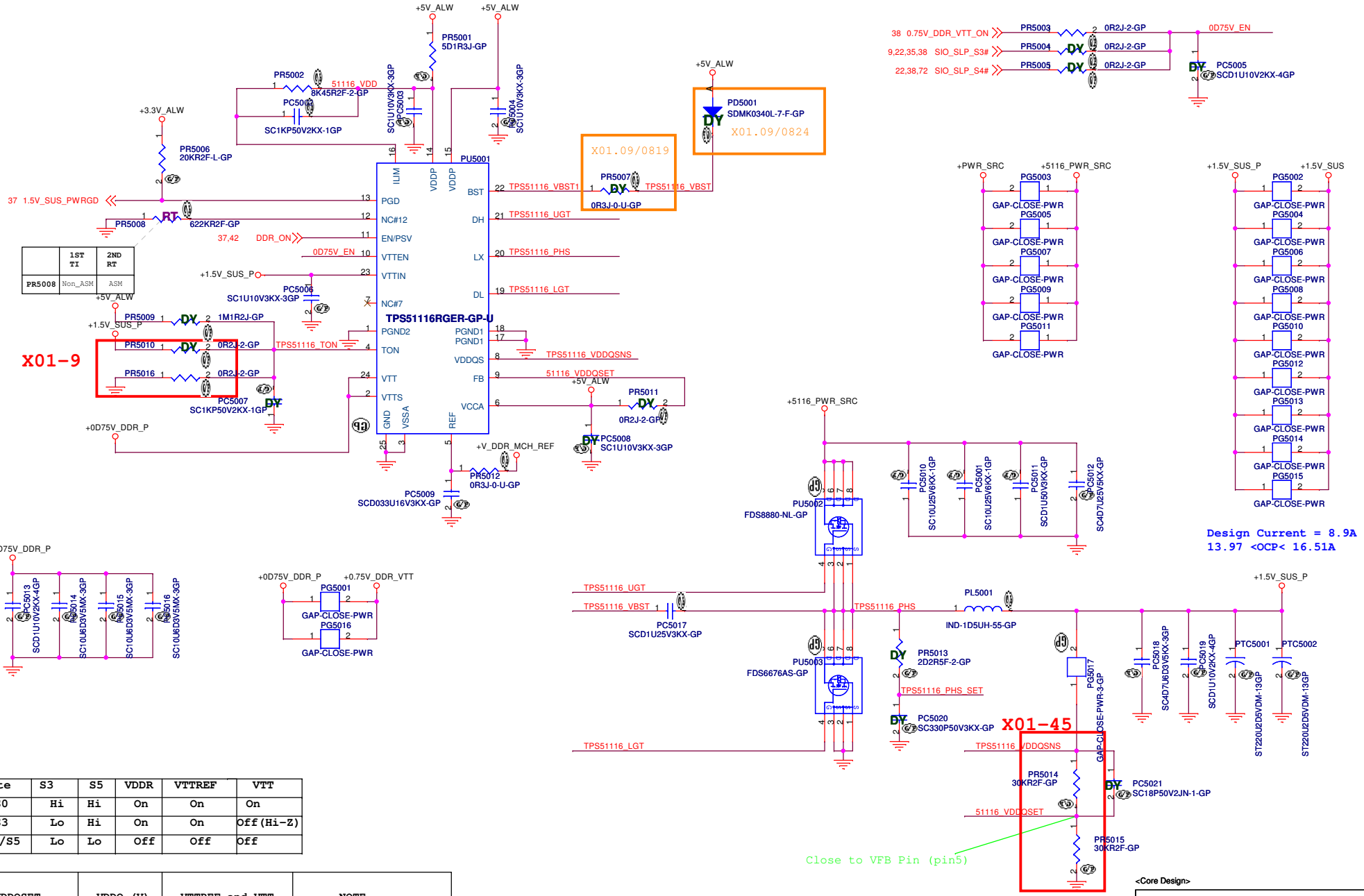
Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 49 of 82

http://sualaptop365.edu.vn

SSID = PWR.Plane.Regulator_1p5v0p75v

www.rosefix.com



	1ST TI	2ND RT
PR5008	Non_ASM	ASM

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDV1040-1R5M=P3 TOKO DCR:3.86 mohm Isat =19.7Arms 68.1R510.10Q
O/P cap: TLPSLV0G227M(25)12RE 25mOhm 2.5Arms NEC_TOKIN/ 77.C2271.07L
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
Switching freq-->400KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.5V / 0.75V

Size: Custom | Document Number: Fonseca UMA | Rev: X01

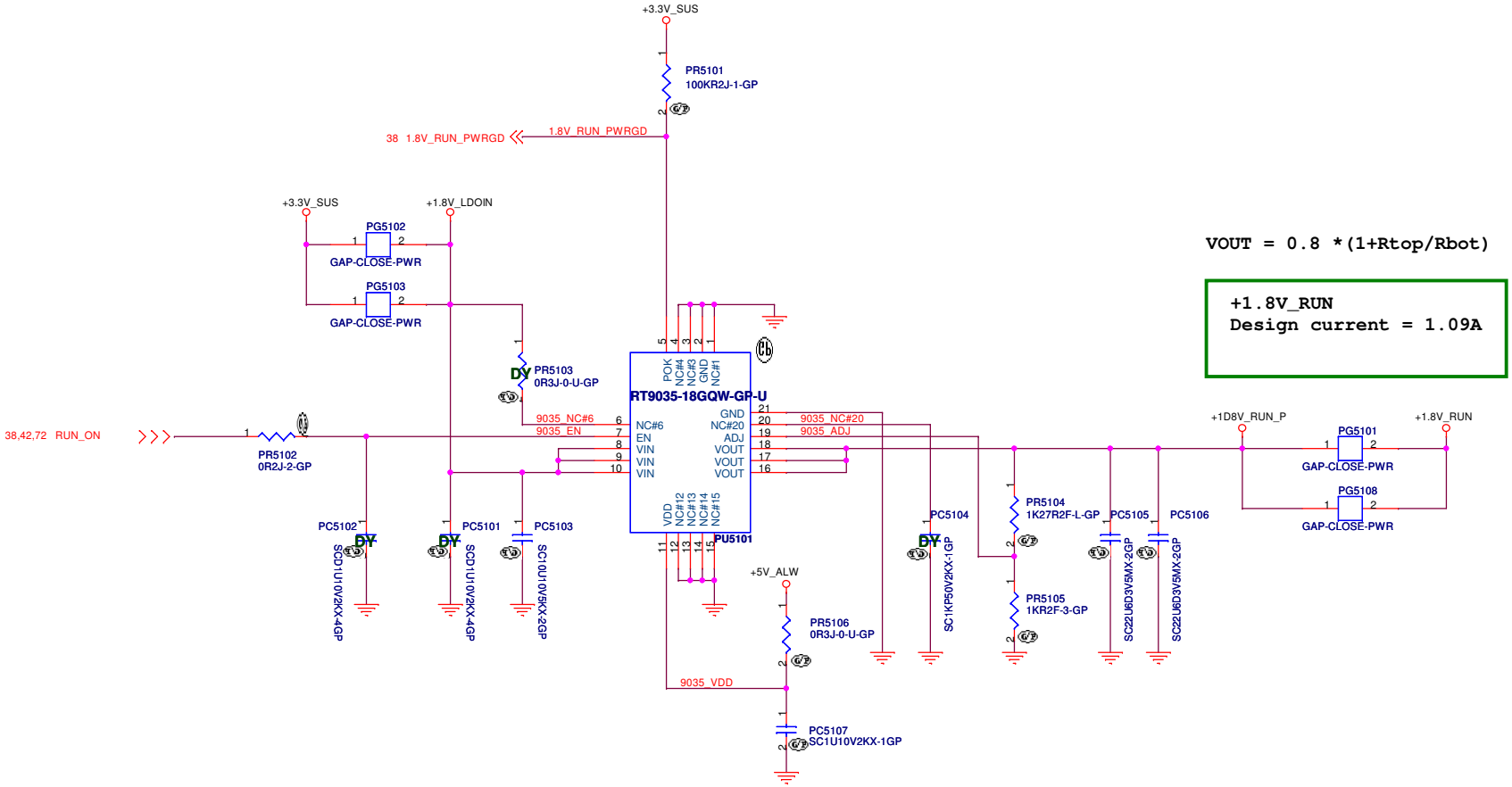
Date: Thursday, October 29, 2009 | Sheet 50 of 82

http://sualaptop365.edu.vn

SSID = PWR.Plane.Regulator_1p8v

LDO for +1.8V_RUN

www.fosefix.com



VOUT = 0.8 *(1+Rtop/Rbot)

+1.8V_RUN
Design current = 1.09A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

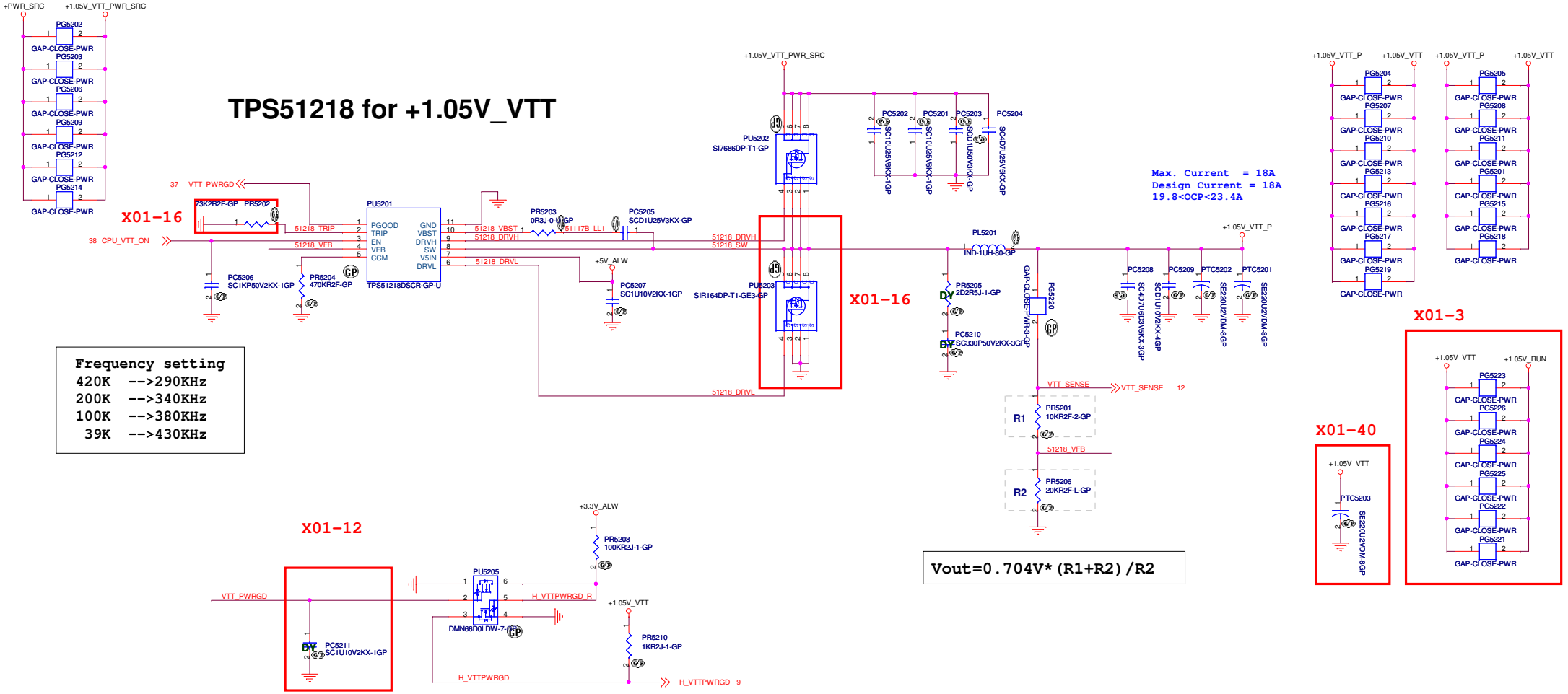
Title	DC to DC +1.8V_RUN	
Size A3	Document Number Fonseca UMA	Rev X01
Date: Thursday, October 29, 2009	Sheet 51 of 82	

http://sualaptop365.edu.vn

SSID = PWR.Plane_Regulator_1p05v

www.fosefix.com

TPS51218 for +1.05V_VTT



Frequency setting
420K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC +1.05V_VTT

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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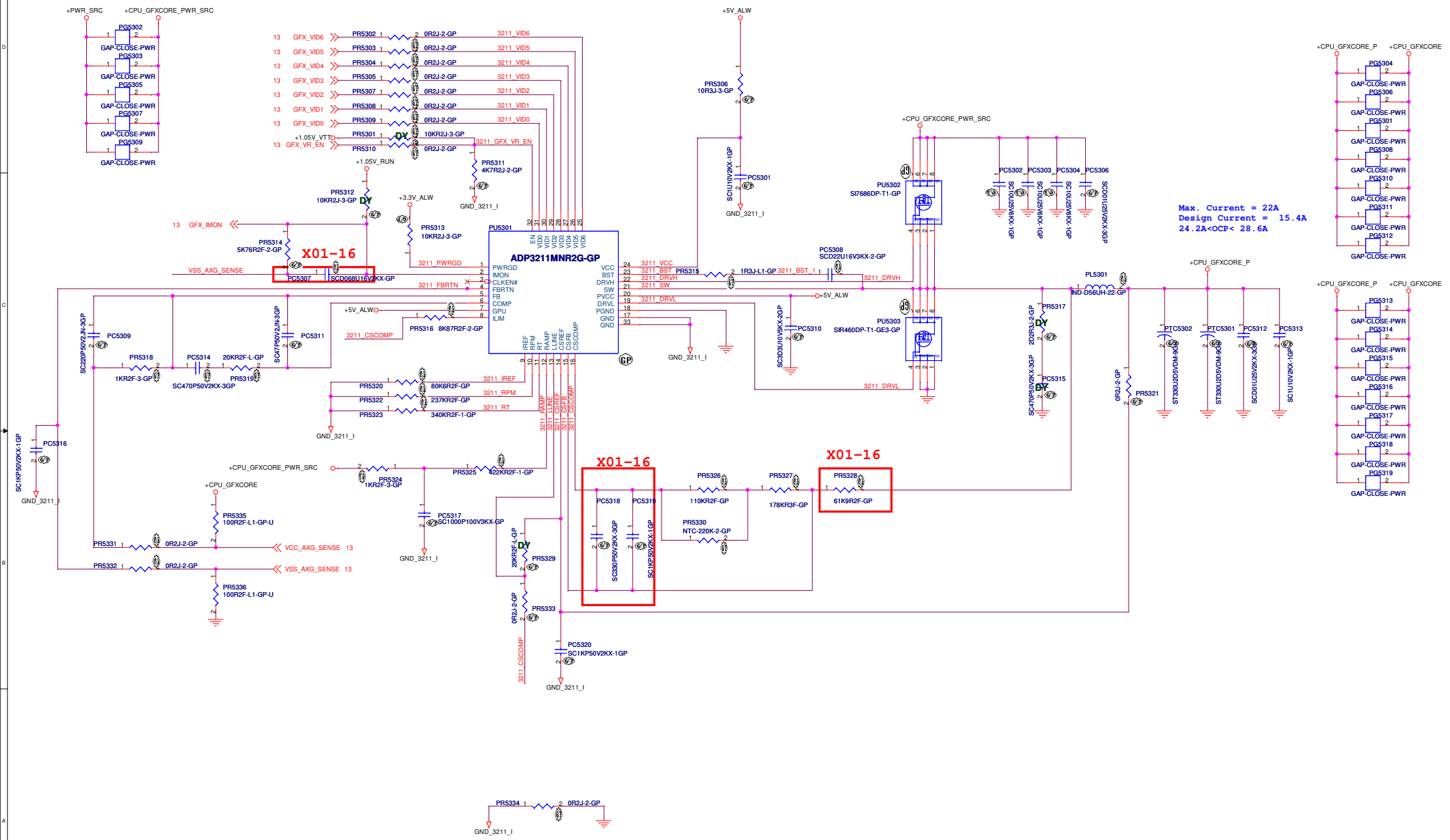
http://sualaptop365.edu.vn

SSID = CPU.GFX.Regulator

www.rosefix.com



http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU_GFXCORE

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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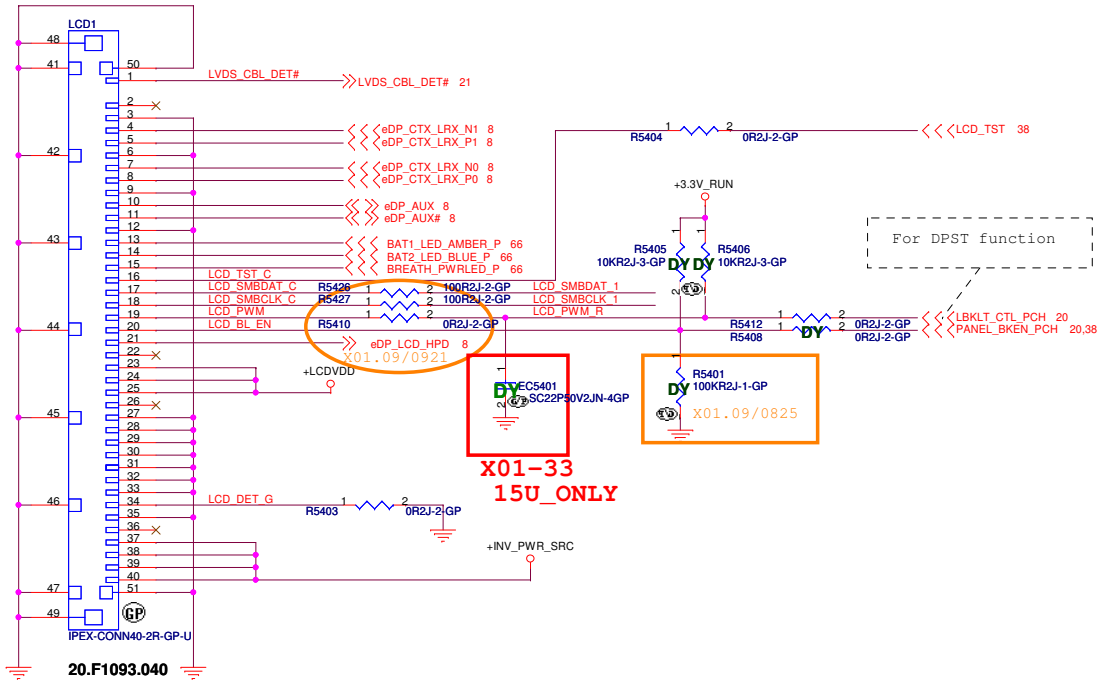
www.rosefix.com

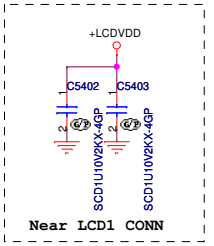
SSID = VIDEO

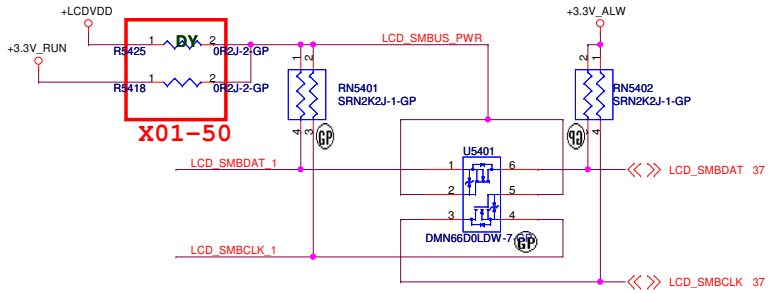
LED Location from left to right

HDD BATTERY

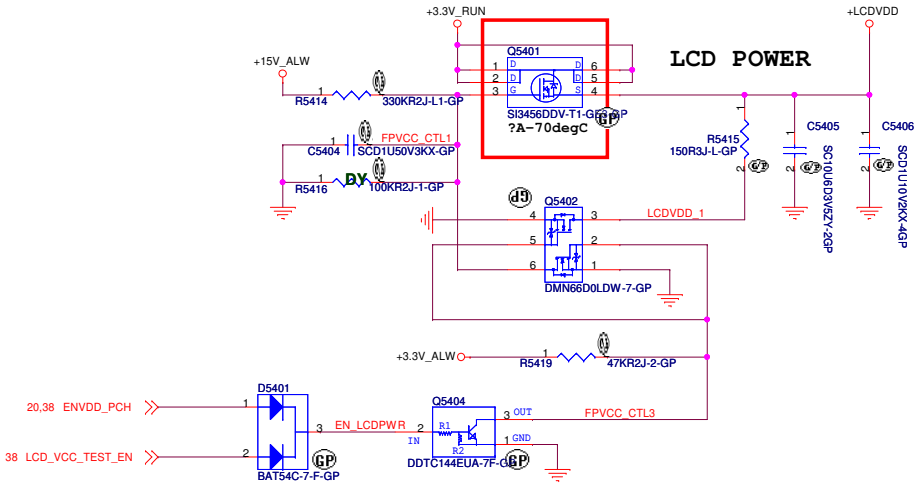


X01.09/0825



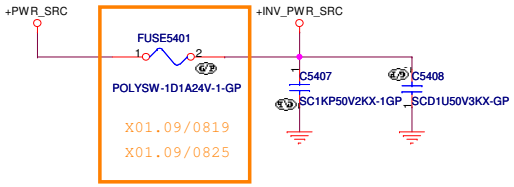


SSID = VIDEO



SSID = Inverter

LED BACKLIGHT CONVERTER POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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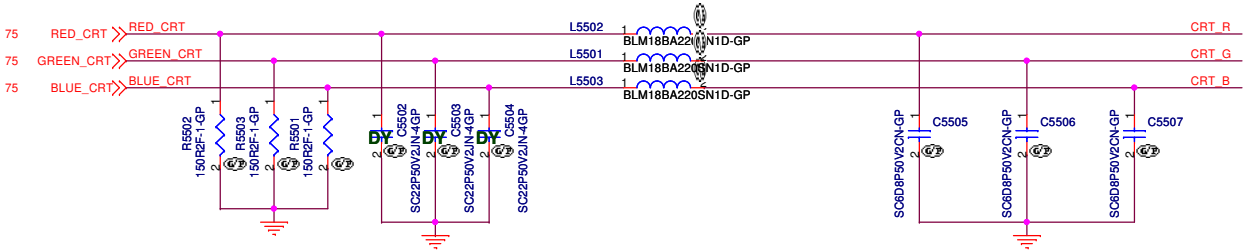
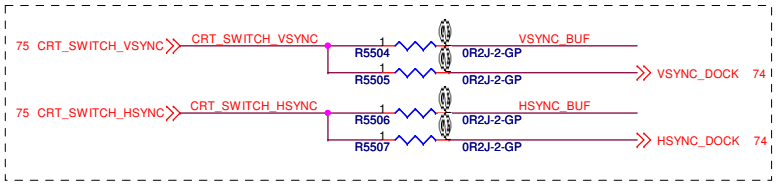
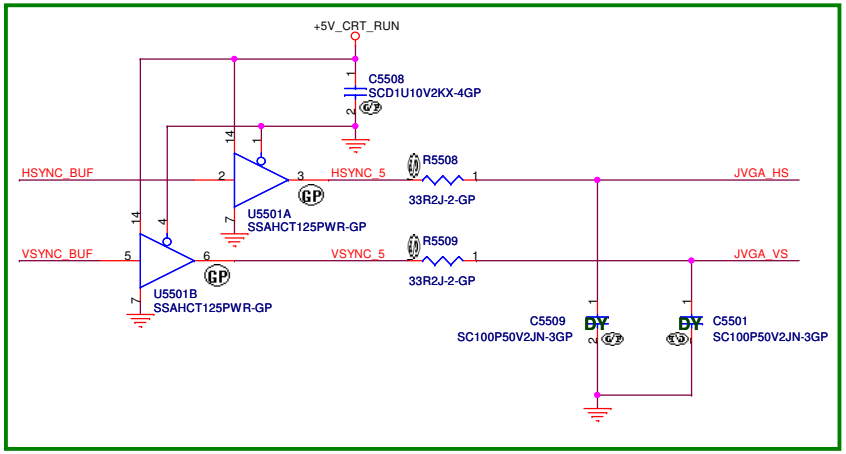
http://sualaptop365.edu.vn

SSID = VIDEO

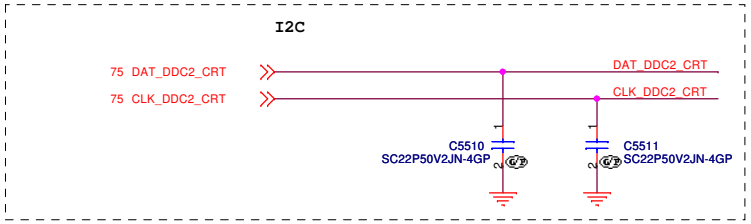
www.rosefix.com



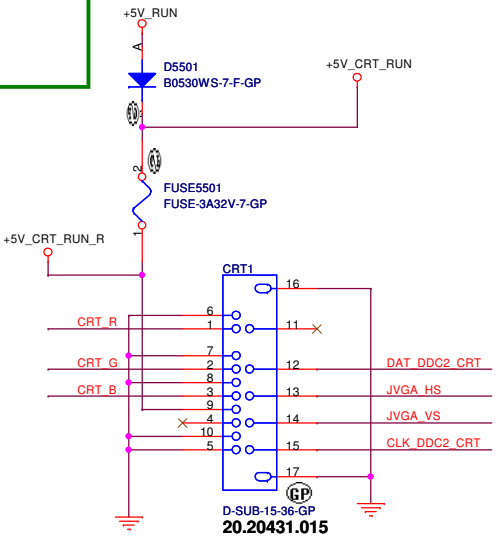




Layout Note:
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



MAX4885E has internal ESD protection and internal level shift



CRT Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT		
Size: A3	Document Number: Fonseca UMA	Rev: X01
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www.rosefix.com

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 56 of 82

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserve*

Size: A3 | Document Number: *Fonseca UMA* | Rev: *X01*

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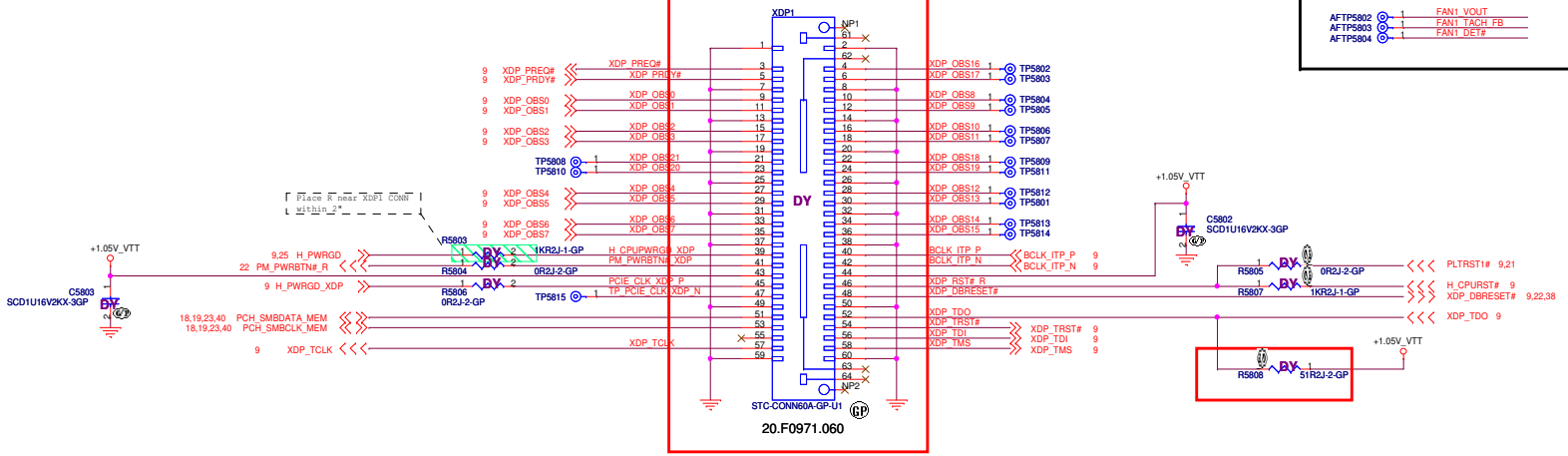
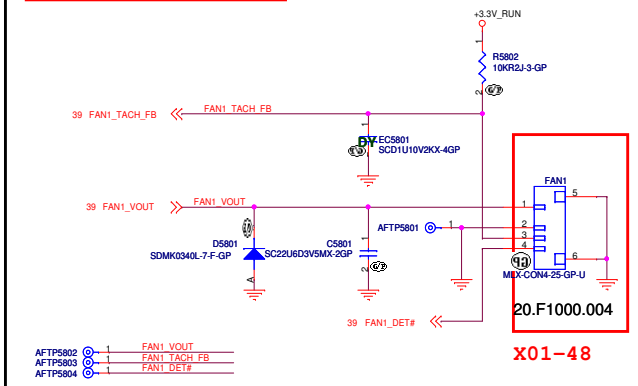
SSID = CPU

X01-7

CPU XDP



SSID = Thermal

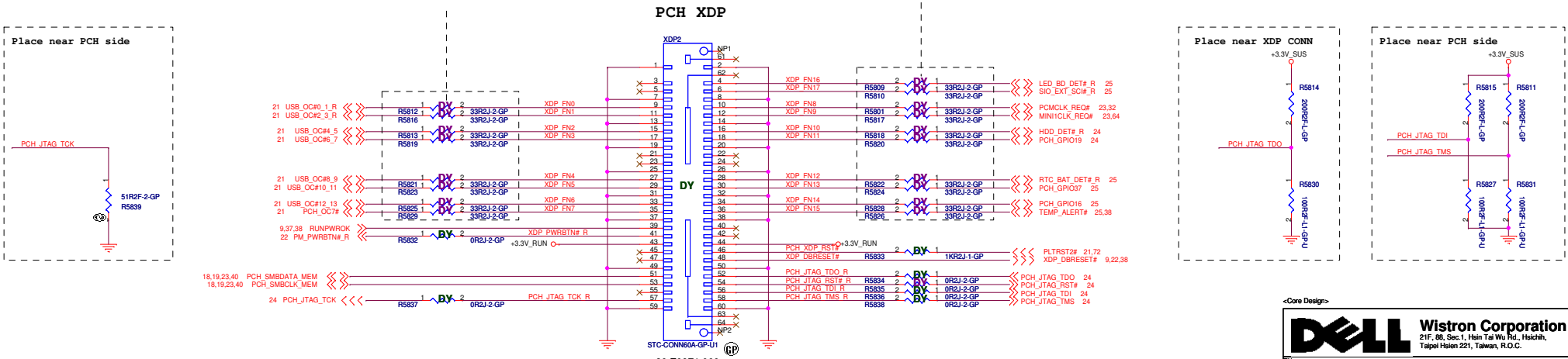


X01-48

SSID = PCH

A 33 ohm series resistor should be placed within 1 inch (or 25.4 mm) of the PCH to source terminate the interface.

PCH XDP



http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size	Document Number	Rev
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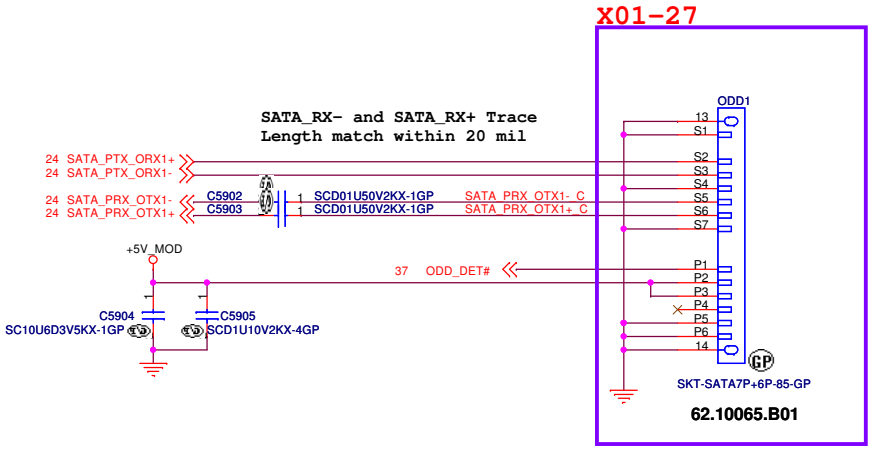
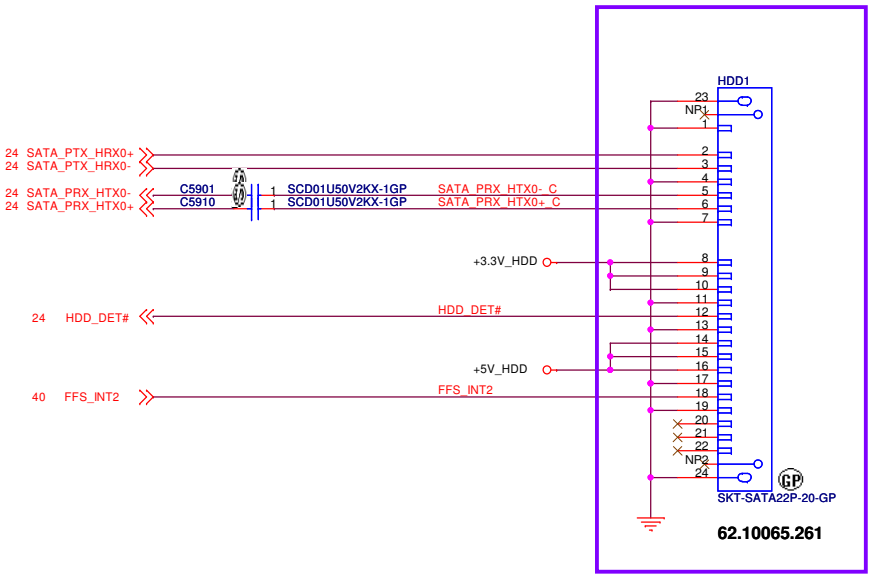
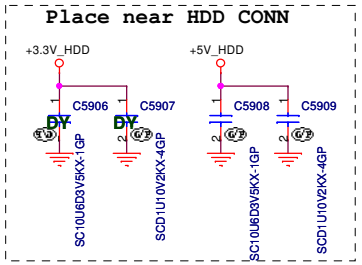
SSID = SATA SATA ODD Connector



SSID = SATA SATA HDD Connector




```
SATA HDD Interface comment
******************************
--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND
******************************
------------ 3.3V
------------ 3.3V
------------ 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
------------ 5V
------------ 5V
------------ 5V
--- GND
(Dell: FFS_INT for supported HDD)
--- GND
------------ 12V (No support)
------------ 12V (No support)
------------ 12V (No support)
******************************
```



http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD / ODD Connector

Size	Document Number	Rev
A3	Fonseca UMA	X01

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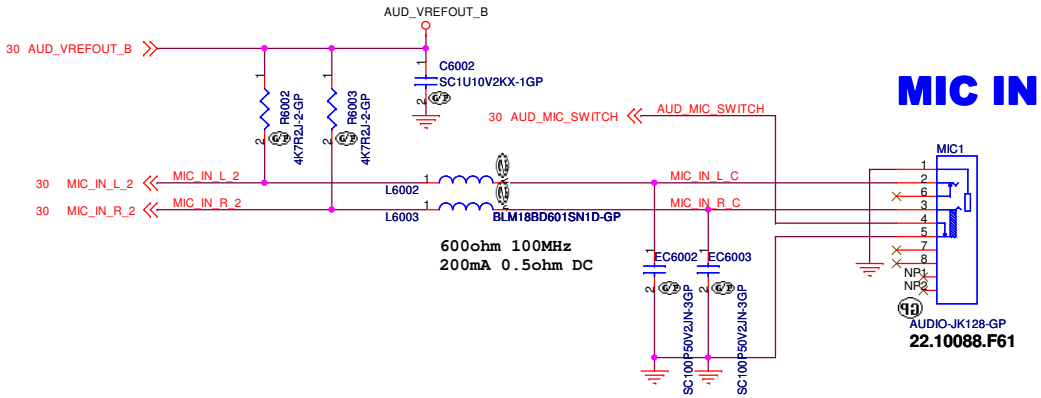
SSID = AUDIO

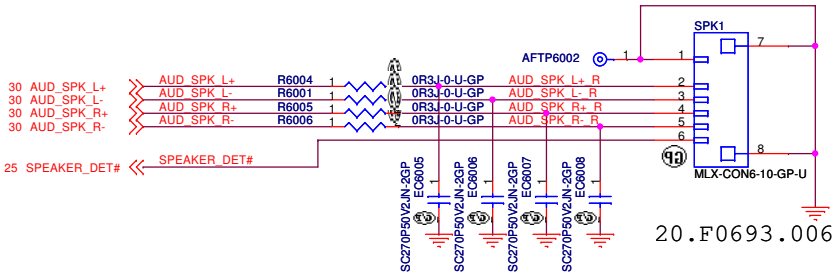
www.rosefix.com

MIC IN



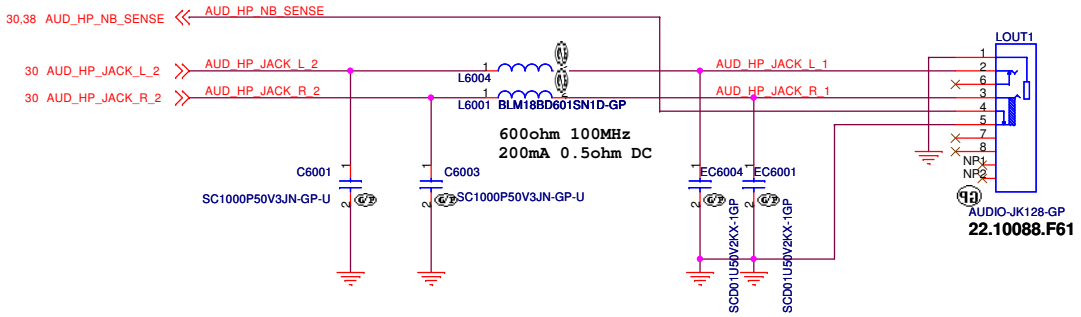
SSID = AUDIO

SPEAKER



SSID = AUDIO

Hear Phone



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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack / Speaker Connector

Size	Document Number	Rev
A3	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 60 of 82

SSID = LOM

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size	Document Number	Rev
C	Fonseca UMA	X01

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SSID = Flash.ROM

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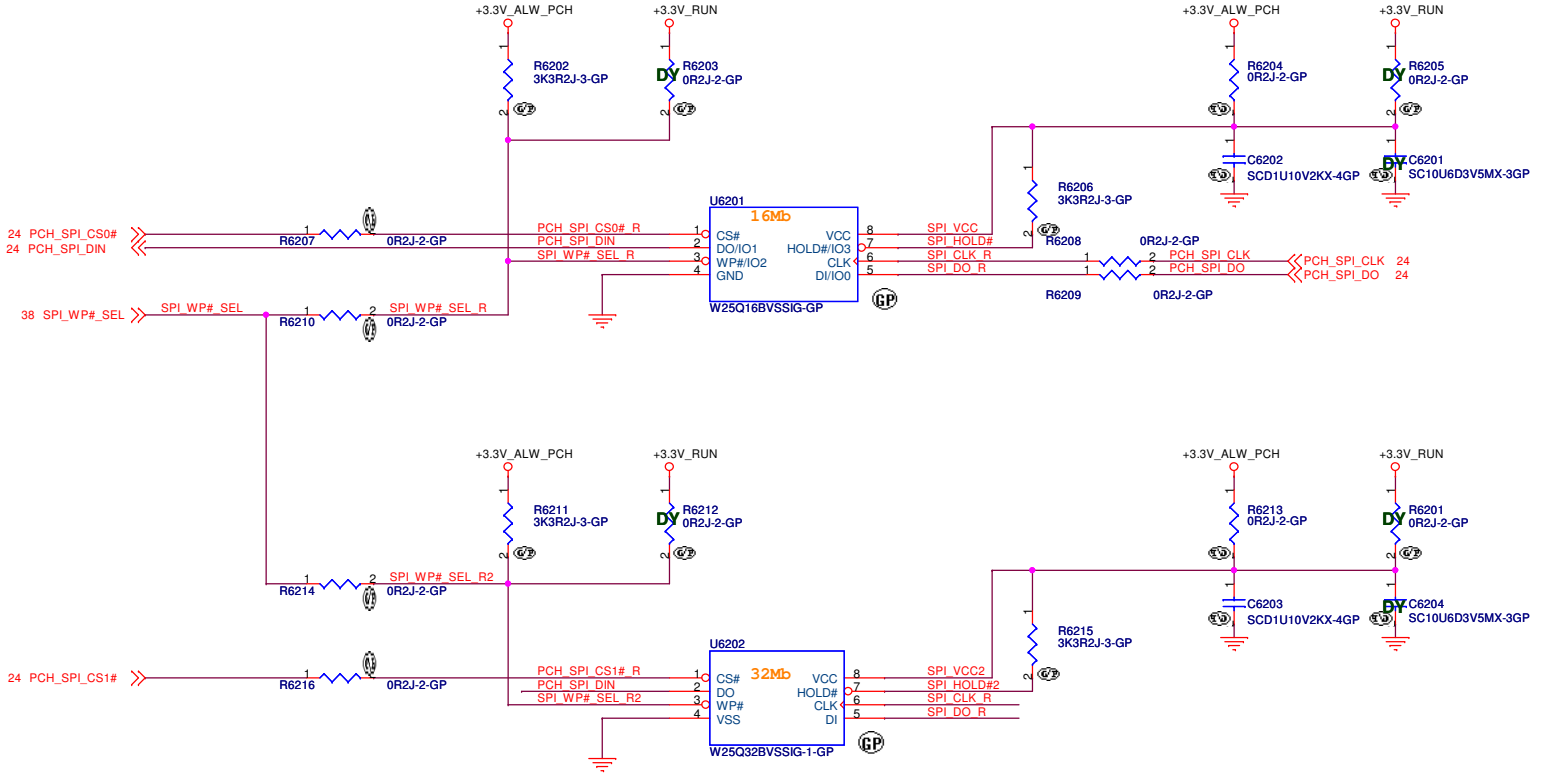
Pin.2
From Intel checklist,
SPI_CS0#/CS1#
No series resistor required
if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)

Pin.6
Intel checklist
No series resistor required if routing length is 1.5"-6.5"
(with 1 or 2 SPI device)



X01-2

#1 source: 72.25Q16.001 (2MB, Winbond)
#2 source: 72.25165.A01 (2MB, MXIC)
#3 source: 72.25016.D01 (2MB, SST)

#1 source: 72.25Q32.A01 (4MB, Winbond)
#2 source: 72.25325.A01 (4MB, MXIC)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash / EEPROM

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SSID = USB

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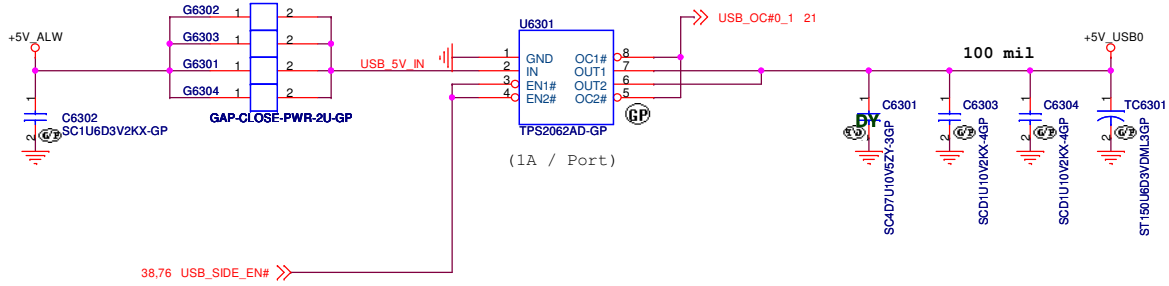
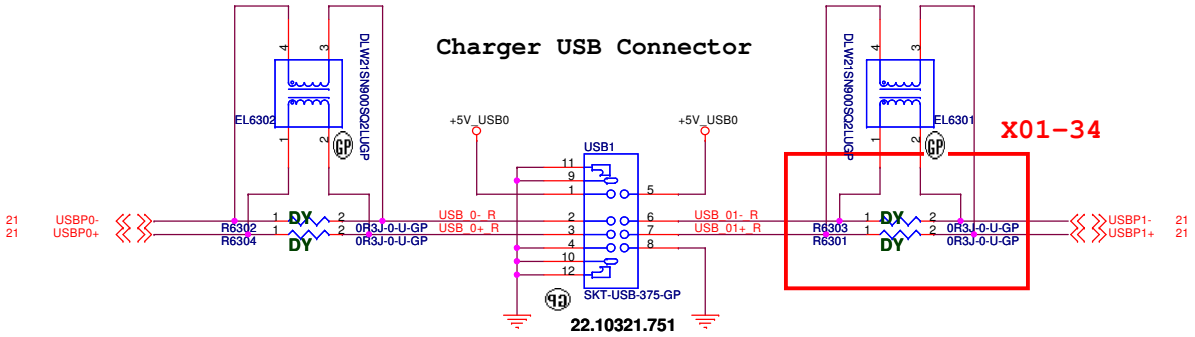
Charger USB

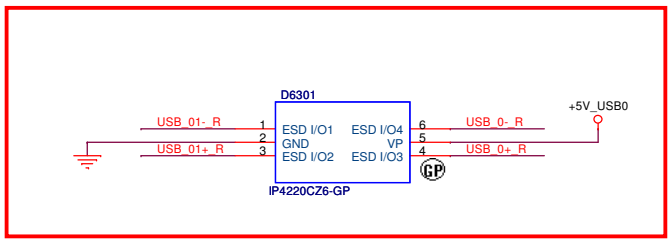


S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

Charger USB Connector



X01-32



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB

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SSID = Wireless

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Near WLAN1, then trace to Pin.2/52/39/41

Near Pin.24

Near WLAN1, then trace to Pin.6/28/48

DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	B44
17	HOST_DEBUG_RX	B46
19	8051_TX	B43
42	8051_RX	A40

MiniCard WLAN connector

X01-5

Debug Only.

62.10043.391

Wireless Switch

WLAN SW (Top View)

OFF ON

62.40083.001

Close WLAN1

http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN / Serial Out Connector

Size: Custom | Document Number: Fonseca UMA | Rev: X01

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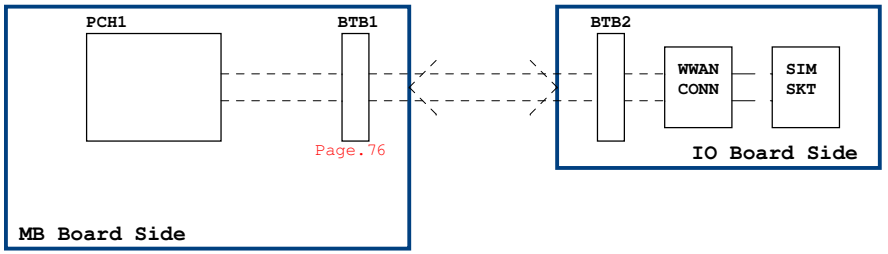
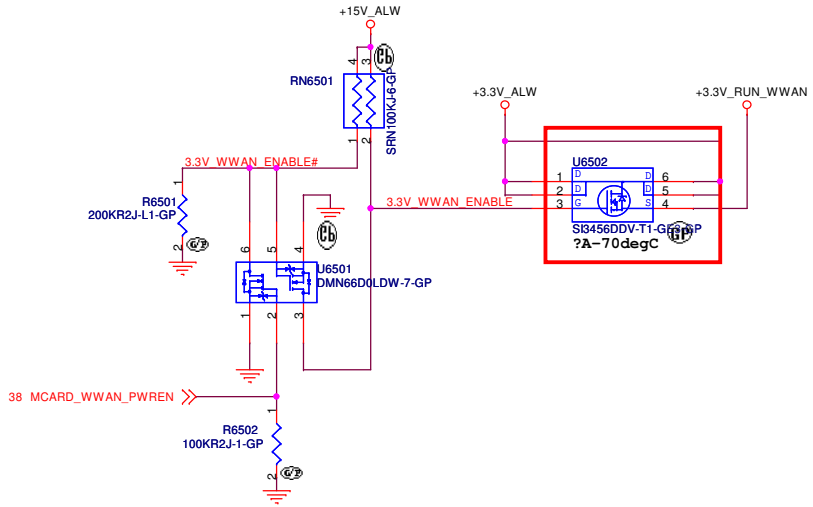
SSID = Wireless

www.rosefix.com





http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN

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SSID = User.interface

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LED Location from left to right
(MB, Top View)

CAPS	NUM	SCRLK
LED6602	LED6603	LED6601

SCRLK LED

38 SCRL_LED# → R6602 20KR2J-L2-GP → SCRL_LED_R# → Q6602 DDTA143ECA-7-F-GP → SCRLK_LED → R6603 680R2J-3-GP → LED_SCRLK_R → LED6601 LED-B-98-GP

+5V_ALW → Q6602 C; EC6602 SCD1U10V2KX-4GP (DY)

CAPS LED

38 CAP_LED# → R6605 20KR2J-L2-GP → CAP_LED_R# → Q6605 DDTA143ECA-7-F-GP → CAP_LED → R6606 680R2J-3-GP → LED_CAP_R → LED6602 LED-B-98-GP

+5V_ALW → Q6605 C; EC6603 SCD1U10V2KX-4GP (DY)

NUM LED

38 NUM_LED# → R6607 20KR2J-L2-GP → NUM_LED_R# → Q6606 DDTA143ECA-7-F-GP → NUM_LED → R6608 680R2J-3-GP → LED_NUM_R → LED6603 LED-B-98-GP

+5V_ALW → Q6606 C; EC6605 SCD1U10V2KX-4GP (DY)

BREATH POWER LED

37,74 BREATH_LED# → Q6603 2N7002A-7-GP (+3.3V_SUS) → BREATH_PWRLED_R# → Q6604 DDTA143ECA-7-F-GP → BREATH_PWRLED_R → R6624 120R2J-2-GP → BREATH_PWRLED_B 76

BREATH_PWRLED_R → R6604 330R2J-3-GP → BREATH_PWRLED_P 54

+5V_ALW → Q6604 C; EC6601 SCD1U10V2KX-4GP (DY)

HDD LED

24 SATA_ACT#_R → R6609 20KR2J-L2-GP → SATA_ACT_C# → Q6607 DDTA143ECA-7-F-GP → HDD_LED → R6610 1KR2J-1-GP → HDD_LED_B 77

+5V_RUN → Q6607 C; EC6604 SCD1U10V2KX-4GP (DY)

WIMAX LED

+3.3V_WLAN → R6615 100KR2J-1-GP (DY) → 64 WIMAX_LED# → D6603 SDMK0340L-7-F-GP

WWAN LED

+3.3V_RUN → R6613 100KR2J-1-GP (DY) → 76 LED_WWAN_OUT# → D6602 SDMK0340L-7-F-GP (14ONLY)

X01-5

WLAN LED

+3.3V_WLAN → R6614 100KR2J-1-GP (DY) → 64 LED_WLAN_OUT# → D6601 SDMK0340L-7-F-GP → R6617 20KR2J-L2-GP → LED_WLAN_OUT_R# → Q6609 DDTA143ECA-7-F-GP → LED_WAN_OUT_R → R6618 1KR2J-1-GP → LED_WLAN_OUT_B 77

+5V_RUN → Q6609 C; EC6608 SCD1U10V2KX-4GP (DY)

Bluetooth LED

73 BT_ACTIVE_K# → R6611 20KR2J-L2-GP → BT_ACT_K_R# → Q6608 DDTA143ECA-7-F-GP → BT_LED_R → R6612 1KR2J-1-GP → BT_LED_B 77

+5V_RUN → Q6608 C; EC6606 SCD1U10V2KX-4GP (DY)

Battery LED (Blue)

37 BAT2_LED# → R6619 10KR2J-3-GP → BAT2_LED_R# → Q6610 DDTA143ECA-7-F-GP → BAT2_LED → R6601 1KR2J-1-GP → BAT2_LED_BLUE_B → BAT2_LED_BLUE_B 77

BAT2_LED → R6620 330R2J-3-GP → BAT2_LED_BLUE_P → BAT2_LED_BLUE_P 54

+5V_ALW → Q6610 C; EC6609 SCD1U10V2KX-4GP (DY)

Battery LED (Amber)

37 BAT1_LED# → R6622 10KR2J-3-GP → BAT1_LED_R# → Q6611 DDTA143ECA-7-F-GP → BAT1_LED → R6621 1KR2J-1-GP → BAT1_LED_AMBER_B → BAT1_LED_AMBER_B 77

BAT1_LED → R6623 1KR2J-1-GP → BAT1_LED_AMBER_P → BAT1_LED_AMBER_P 54

+5V_ALW → Q6611 C; EC6610 SCD1U10V2KX-4GP (DY)

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: LED

Size	Document Number	Rev
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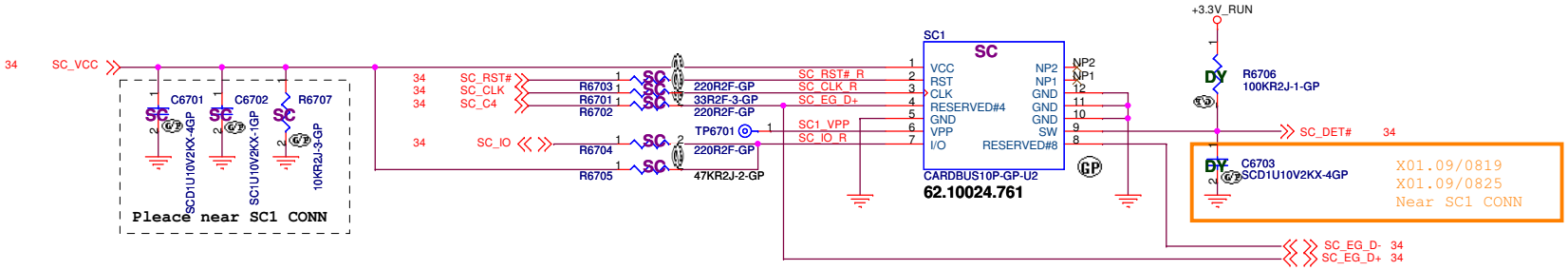
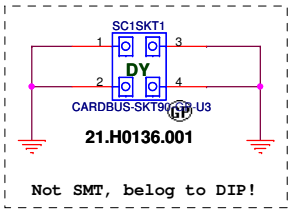
SSID = SmartCard

www.rosefix.com

SmartCard



SmartCard Socket



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Smart Card Socket

Size: A3 | Document Number: Fonseca UMA | Rev: X01

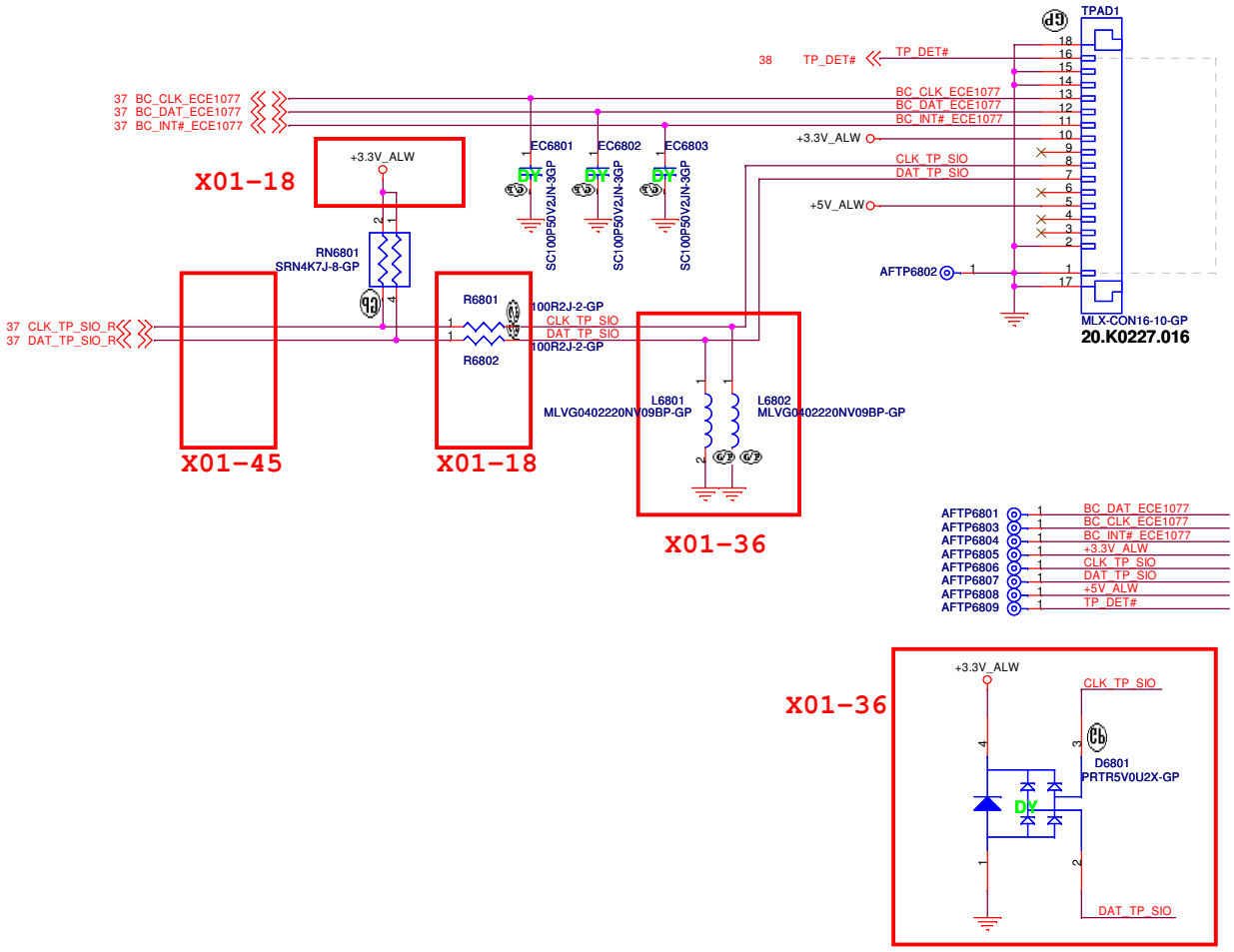
Date: Thursday, October 29, 2009 | Sheet 67 of 82

http://sualaptop365.edu.vn

SSID = Touch.Pad

www.rosefix.com

TouchPad Connector



Touch PAD Module Side

16	TP_DET#
15	GND
14	GND
13	BC_CLK (ECE1077)
12	BC_DAT (ECE1077)
11	BC_INT# (ECE1077)
10	3.3V_ALW
09	3.3V_RUN (Internal NC)
08	PS2_CLK
07	PS2_DATA
06	5V_RUN (Backlight, No Use)
05	5V_ALW (Chip change to use 3V, NC)
04	PWM (Backlight, No Use)
03	GND (Backlight, No Use)
02	GND
01	Diag_loop

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch Pad Connector

Size: A3 | Document Number: Fonseca UMA | Rev: X01

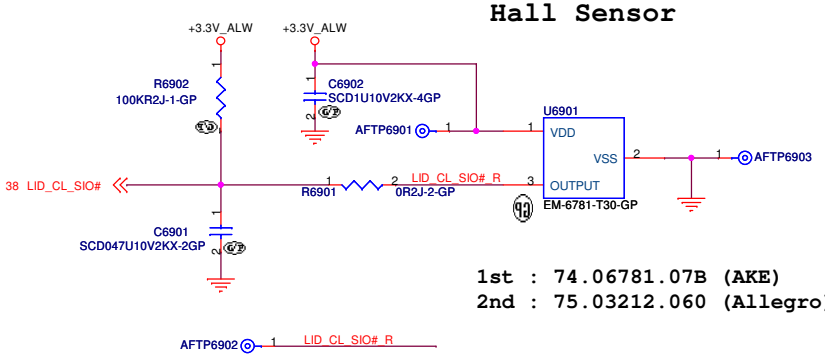
Date: Thursday, October 29, 2009 | Sheet 68 of 82

http://sualaptop365.edu.vn

SSID = User.interface

www.fosefix.com

Hall Sensor



1st : 74.06781.07B (AKE)
2nd : 75.03212.060 (Allegro)

http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

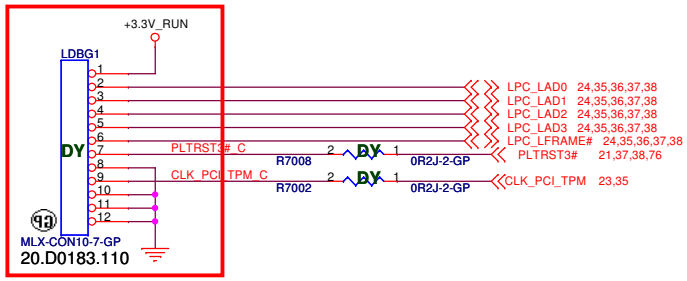
Title		
Hall Sensor		
Size: A3	Document Number: Fonseca UMA	Rev: X01
Date: Thursday, October 29, 2009	Sheet 69 of 82	

SSID = User.Interface

www.fosefix.com

LPC Debug port

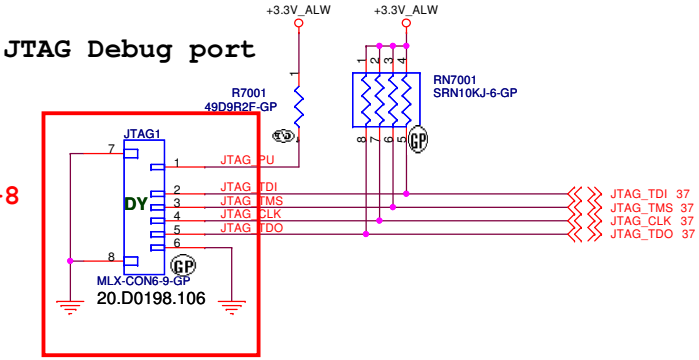
X01-8

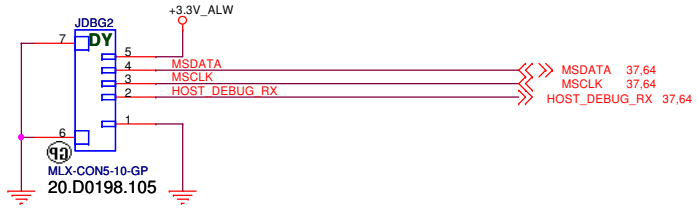


LDBG1, need pop R7008, R7002

JTAG Debug port

X01-8





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: JTAG Debug

Size: A3 | Document Number: Fonseca UMA | Rev: X01

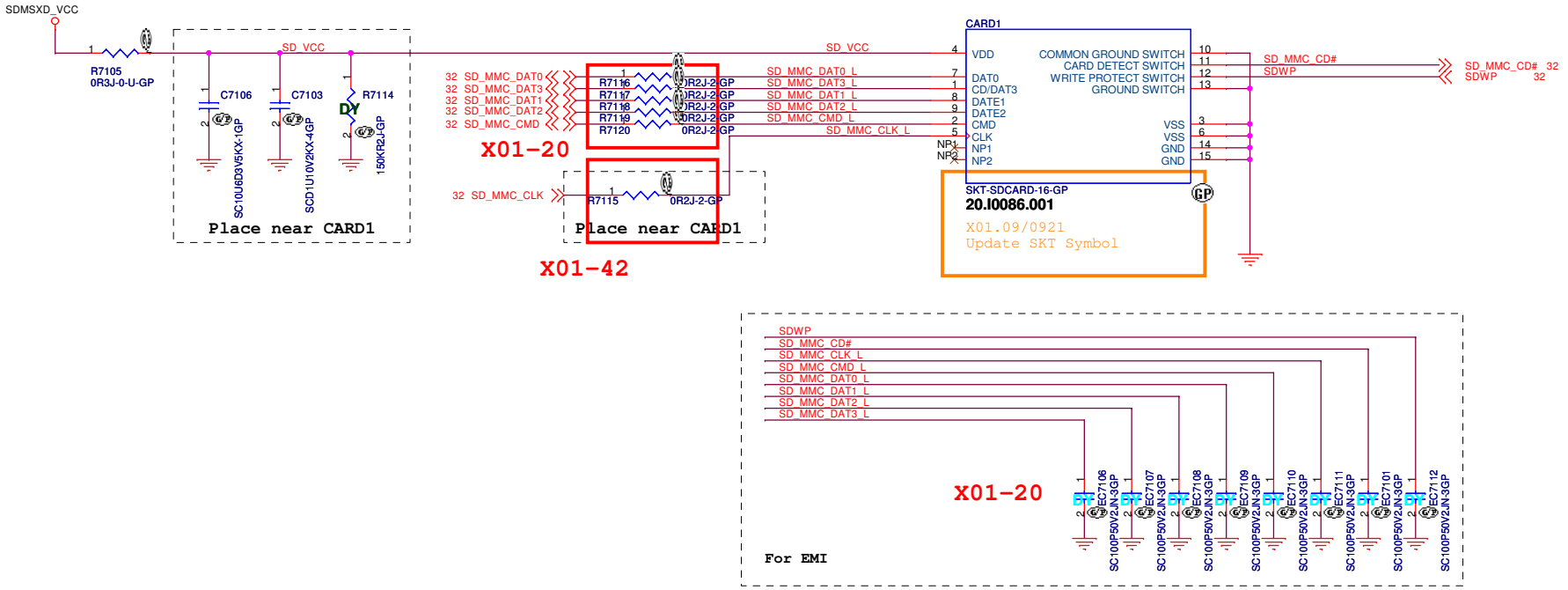
Date: Thursday, October 29, 2009 | Sheet 70 of 82

http://sualaptop365.edu.vn

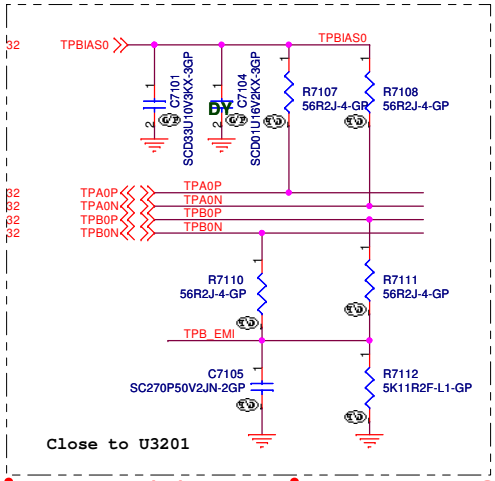
www.rosefix.com

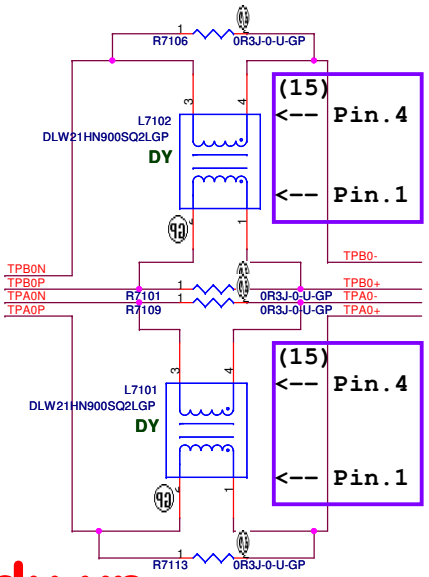
SSID = 1394

Flash Reader Socket

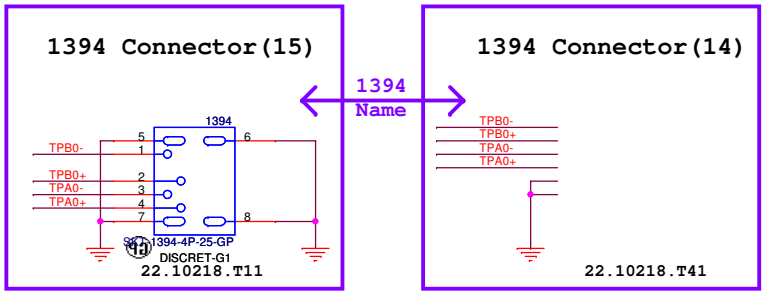


SSID = 1394





Shield GND separately for pairs of
TPA+ & TPA- and TPB+ & TPB-



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1394 Connector / Flash Socket
Size: A3 | Document Number: Fonseca UMA | Rev: X01
Date: Tuesday, November 03, 2009 | Sheet 71 of 82

http://sualaptop365.edu.vn

www.rosefix.com

SSID = CARDBUS

Cardbus Connector

CBS_CCD1# CBS_CCD2#

C7202 SC270P50V2JN-2GP C7203 SC270P50V2JN-2GP

Close to Socket

CBS_CAD13, CBS_CAD15 Can be used as Express Card USB differential pair.

CBS_CAD[0..31] 32

CBUS1 — PCC

FOX-CONN84-GP 62.10024.981

+CBS_VCC +CBS_VPP

C7204 SCD01U16V2KX-3GP C7201 SCD01U16V2KX-3GP C7205 SC10U6D3V5KX-1GP

Close to Socket

C7206 SCD1U10V2KX-4GP

Close to Socket

Cardbus Shocket

PCMCIA1 DY

CARDBUS-SKT104-GP-U 21.H0164.001

Not SMT, belog to DIP!

U7201 PCC — R5531V002-GP

C7207 SC1U6D3V2KX-GP C7208 SC1U6D3V2KX-GP C7209 SCD01U16V2KX-3GP C7210 SC10U6D3V5KX-GP

C7211 SCD1U10V2KX-4GP C7212 SCD01U16V2KX-3GP

+CBS_VCC Short Current Limit, 1400mA

+CBS_VPP Short Current Limit, 300mA

SSID = ExpressCard

NewCard Shocket

NEW1SKT1 DY CARD-PUSH-2P-GP-U2 21.H0156.001

Not SMT, belog to DIP!

C7223 C7222 R7204 2K2R2J-2-GP

C7225 C7224 R7205 2K2R2J-2-GP

Place them near to NEW1

NewCard Connector

NEW1 — EXPRESSCARD-26P-14-GP 62.10081.321

PCIE_PTX_EXPRX_P4_C 23 PCIE_PTX_EXPRX_N4_C 23

PCIE_PRX_EXPTX_P4 23 PCIE_PRX_EXPTX_N4 23

CLK_PCIE_EXP 23 CLK_PCIE_EXP# 23

EXPRCRD_CPPE# EXPCLK_REQ# 23

PERST# PCIE_WAKE# PCIE_WAKE# 35,38,64

CARD_SMBDAT 37 CARD_SMBCLK 37

CPUSB# USBP+_EXP USBP-_EXP

R7202 R7203 0R2J-2-GP — Place R near U3201

USBP12+ 21,32,34 USBP12- 21,32,34

X01.09/0819 +3.3V_RUN R7211 10KR2J-3-GP

+3.3V_CARD +3.3V_CARDAUX +1.5V_CARD

RN7201 SRN100KJ-6-GP

U7202 EXP — TPS2231MRGPR-GP

38 EXPRCRD_STDBY# 38,42,51 RUN_ON

21,58 PLTRST2#

C7226 SC22P50V2JN-4GP X01.09/0819

38 EXPRCRD_PWREN# EXPRCRD_CPPE#

22,38,50 SIO_SLP_S4#

EXPRCRD_STDBY# EXPRCRD_RST# PERST# CPUSB# CPPE# EXPRCRD_SHDN#

C7213 C7214 C7215 C7216 C7217 C7218 C7219 C7220

Place them near to U7202

+1.5V_CARD Max. 650mA, Average 500mA.

+3.3V_CARD Max. 1300mA, Average 1000mA

+3.3V_CARDAUX Max. 275mA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / ExpressCard

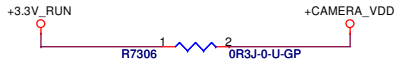
Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 72 of 82

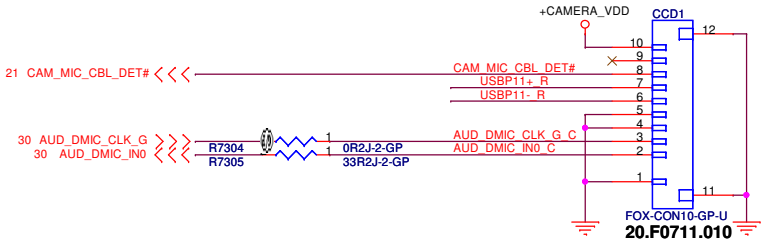
http://sualaptop365.edu.vn

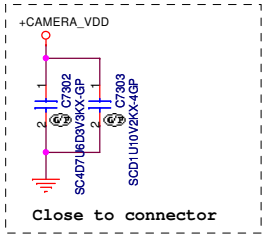
www.rosefix.com

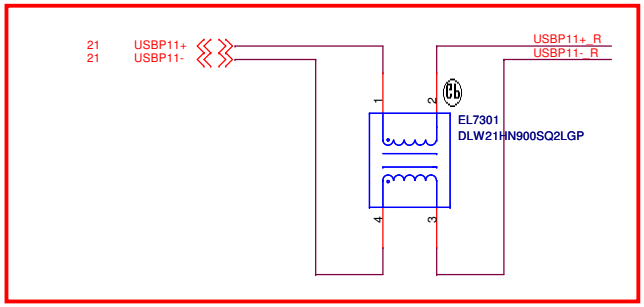
Camera Power CTRL

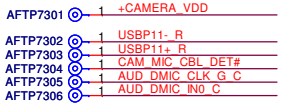


Camera Connector



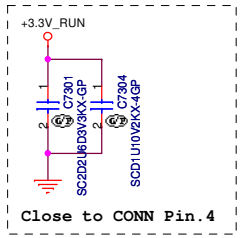


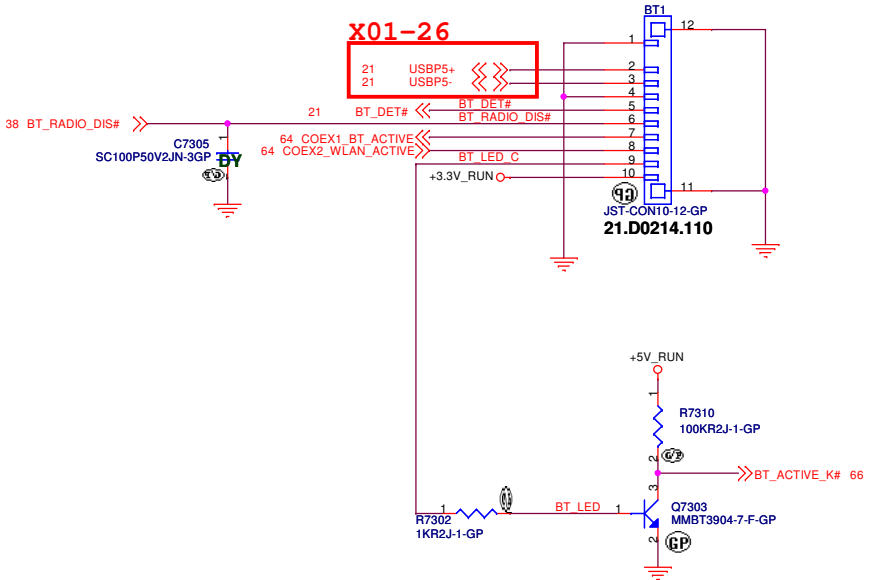


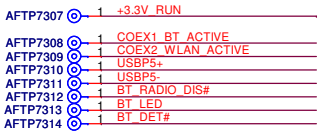


User.interface

Bluetooth Connector







MB BT CONN / BT Module CONN

PIN	Define	PIN	Define
1	GND	1	GND
2	USBP5+_R	12	USB_DP
3	USBP5-_R	11	USB_DN
4	GND	10	GND
5	BT_DET#	2	MOD_DET
6	BT_RADIO_DIS#	7	RADIO_DIS
7	COEX1_BT_ACTIVE	3	COEX1_BT_ACTIVE
8	COEX2_WLAN_ACTIVE	8	COEX2_WLAN_ACT
9	BT_LED	6	LINK_IND
10	+3.3V_RUN	9	3.3V
11	NC		
12	NC		

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth / Camera / DMIC

Size: A3 | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 73 of 82

http://sualaptop365.edu.vn

SSID = Docking

www.rosefix.com

DK1

JAE-CONN144D-3-GP-U

X01-15 20.F1572.144

Dock eSATA

]----->Dock USB 1

]----->Dock USB 2

Clost to DK1

From GPU

From GPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Docking Connector

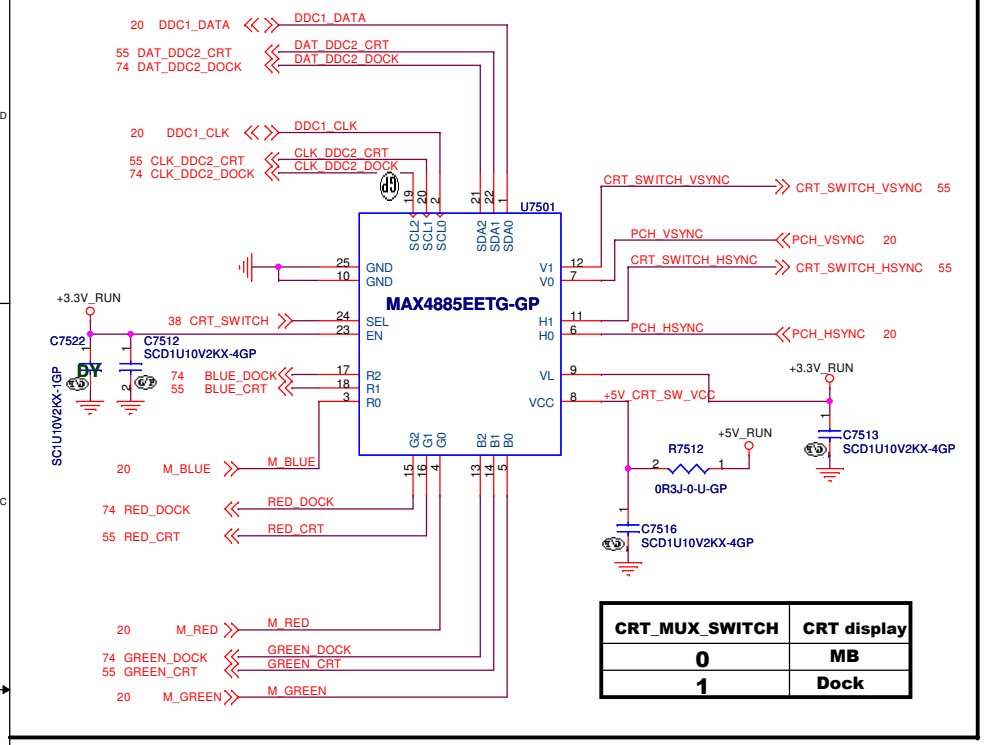
Size: Custom | Document Number: Fonseca UMA | Rev: X01

Date: Thursday, October 29, 2009 | Sheet 74 of 82

http://sualaptop365.edu.vn

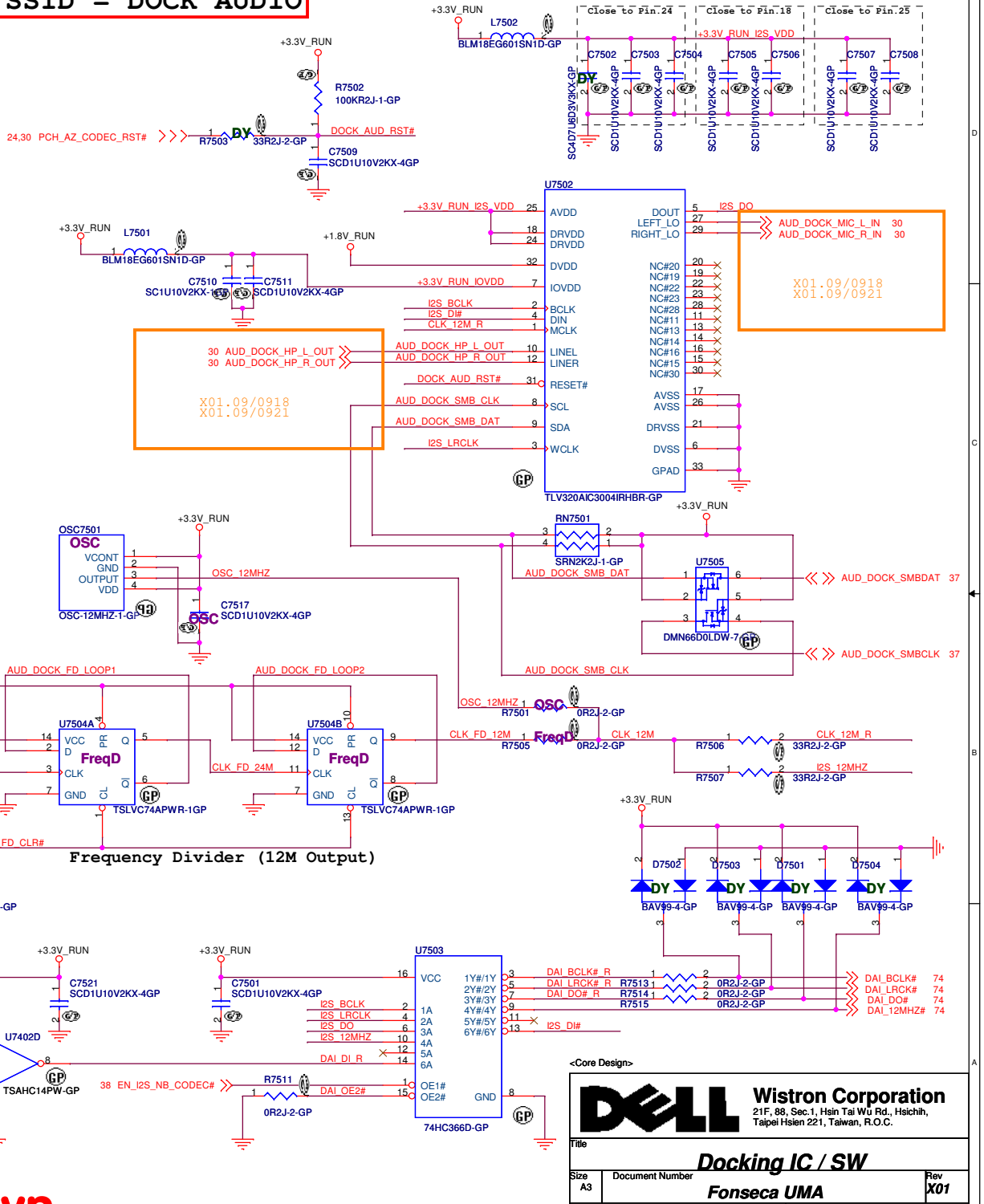
www.fosefix.com

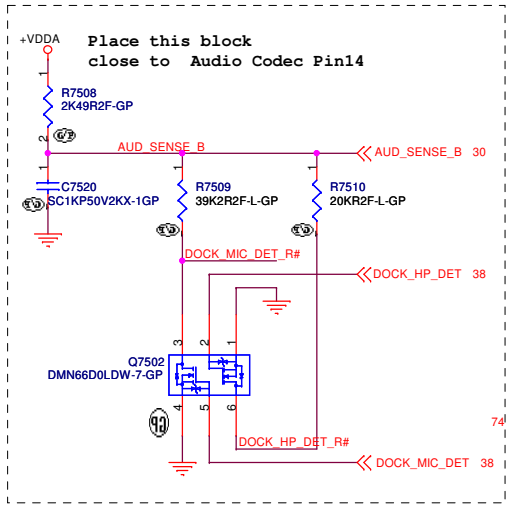
SSID = DOCK CRT SWITCH

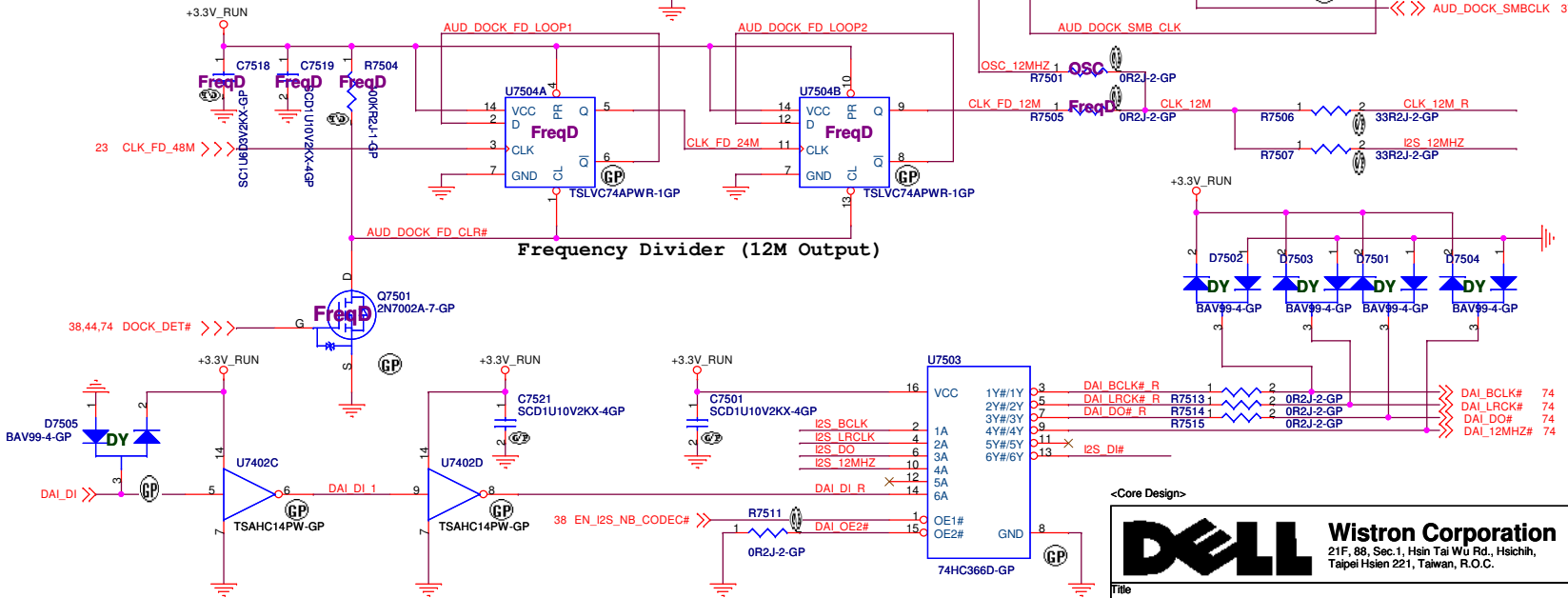


CRT_MUX_SWITCH	CRT display
0	MB
1	Dock

SSID = DOCK AUDIO







http://sualaptop365.edu.vn

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

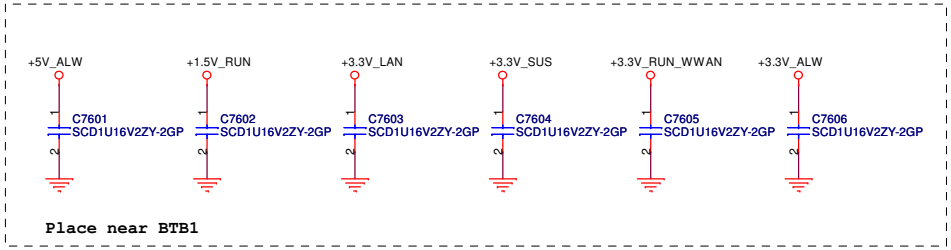
Title: Docking IC / SW

Size: A3 | Document Number: Fonseca UMA | Rev: X01

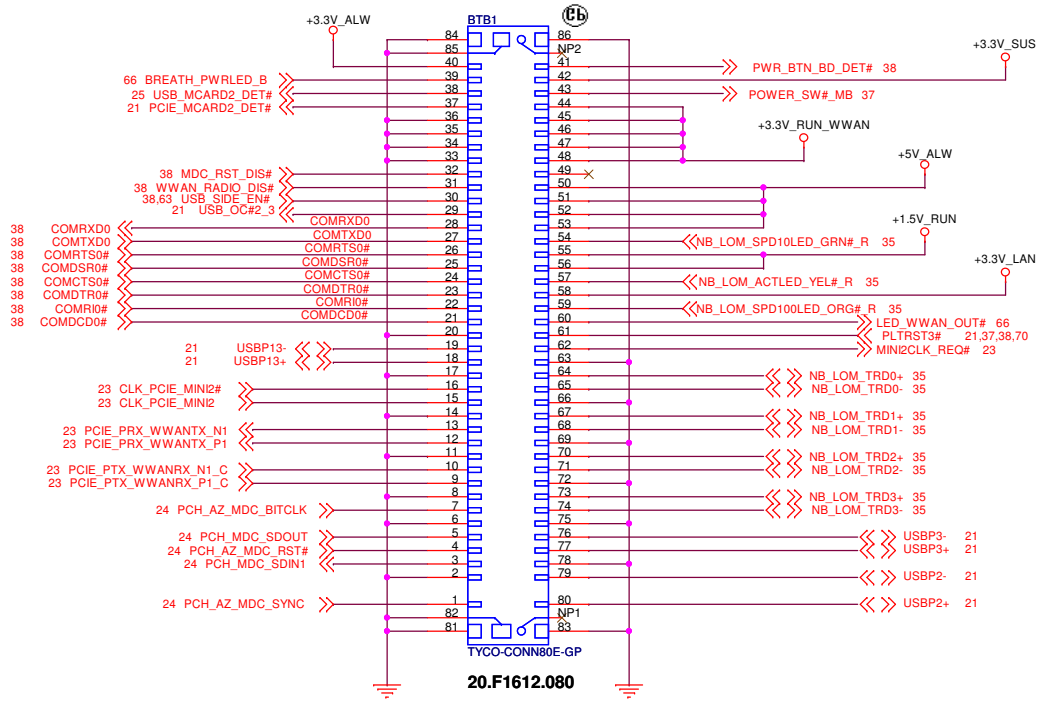
Date: Thursday, October 29, 2009 | Sheet 75 of 82

SSID = User.Interface

www.fosefix.com



IO Board Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board CONN

Size	Document Number	Rev
A3	Fonseca UMA	X01

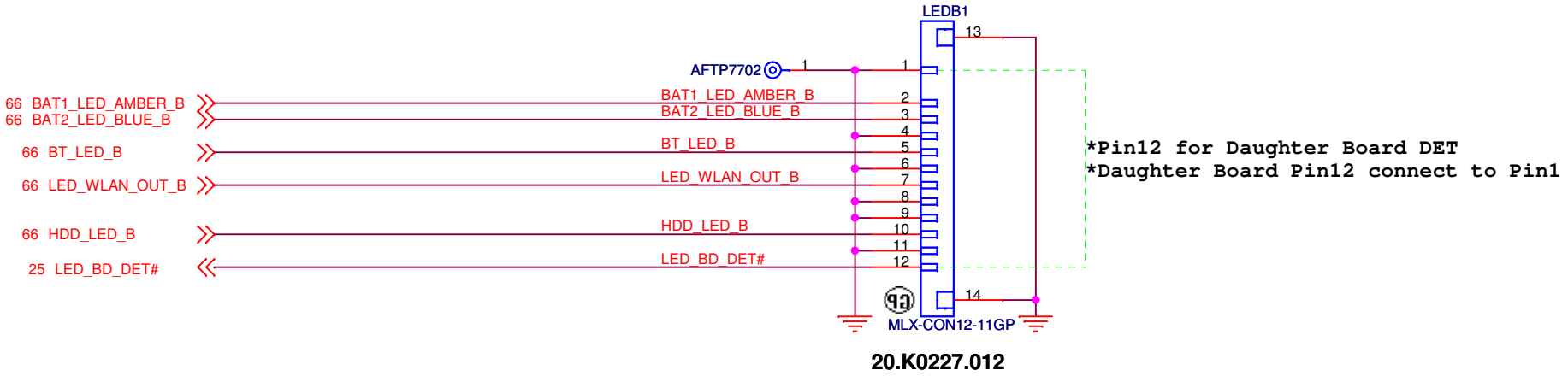
Date: Thursday, October 29, 2009 Sheet 76 of 82

http://sualaptop365.edu.vn

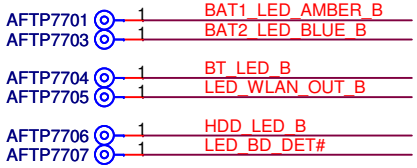
SSID = User.interface

www.rosefix.com

LED BD Connector



20.K0227.012



LED Location from left to right

HDD	BATTERY	WLAN	BLUE TOOTH

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Board Connector

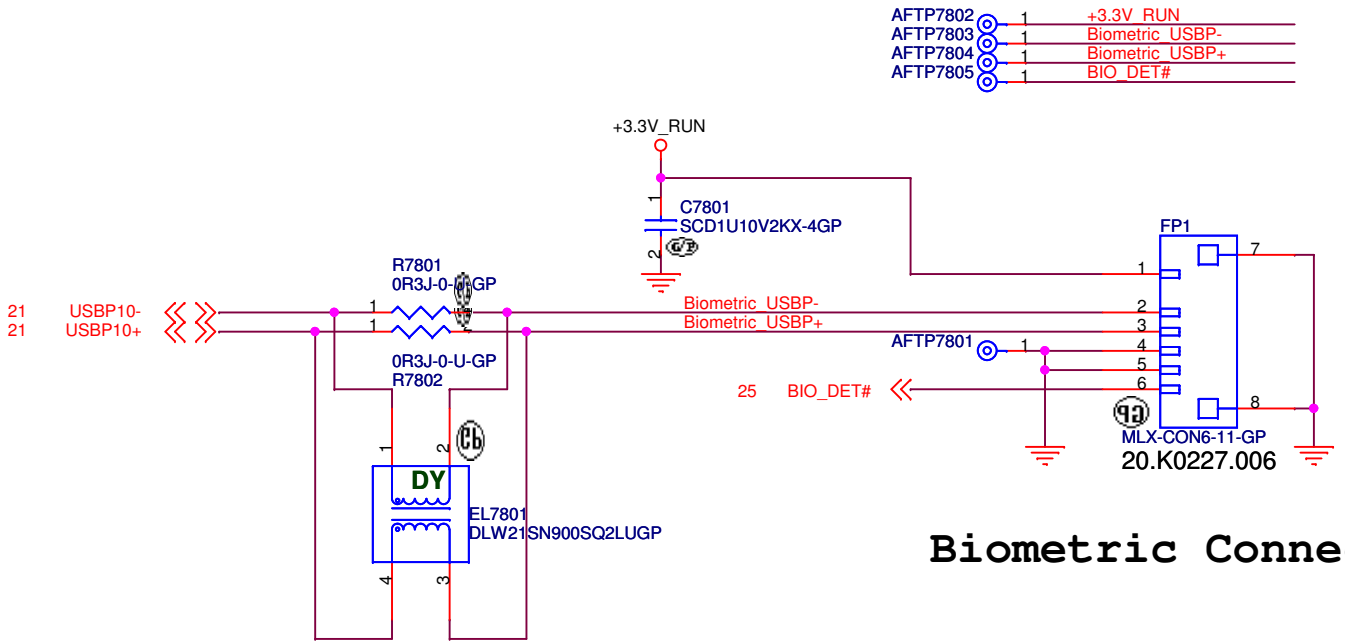
Size	Document Number	Rev
A4	Fonseca UMA	X01

Date: Thursday, October 29, 2009 Sheet 77 of 82

http://sualaptop365.edu.vn

SSID = User.Interface

www.rosefix.com



Biometric Connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Printer Board CONN***

Size	Document Number	Rev
A4	***Fonseca UMA***	***X01***

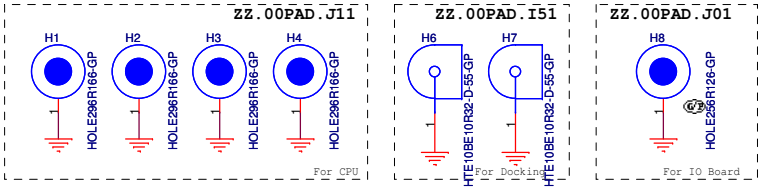
Date: Thursday, October 29, 2009 Sheet 78 of 82

http://sualaptop365.edu.vn

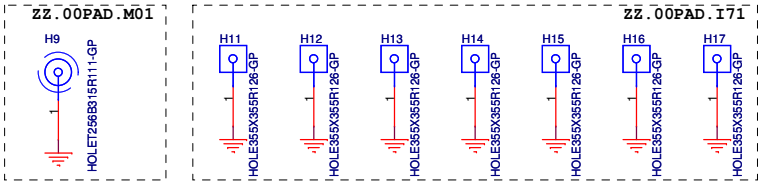
SSID = Mechanical

www.rosefix.com

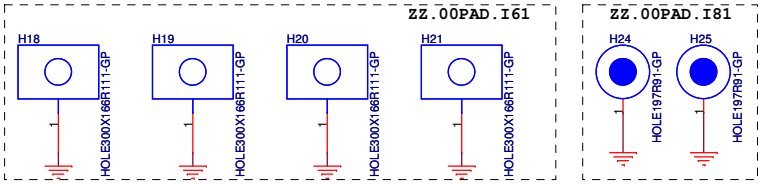
Hole

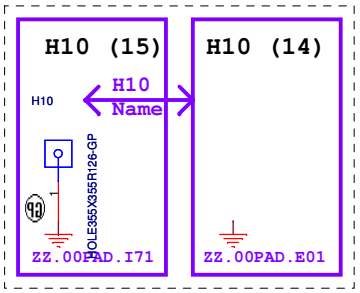


Hole

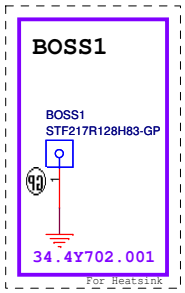


Hole



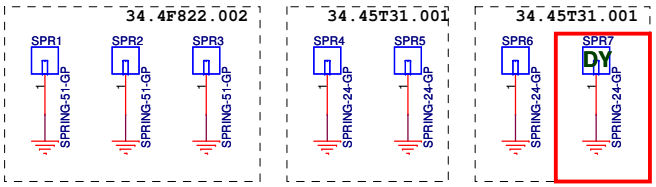


X01-1



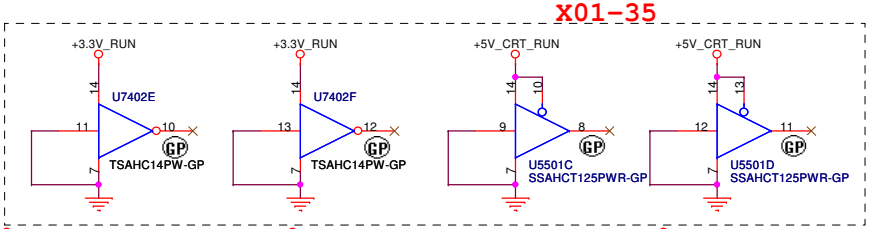
X01-29

Spring

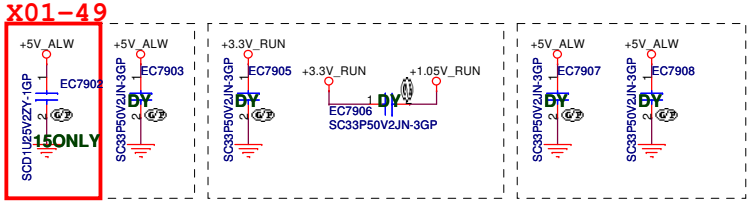


X01-35

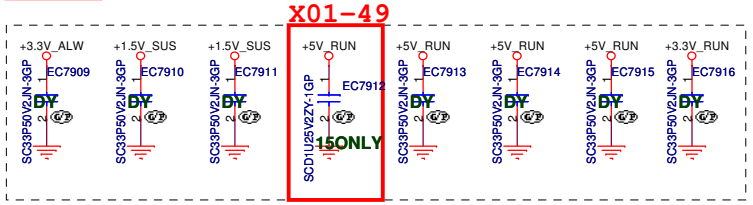
Unused Parts



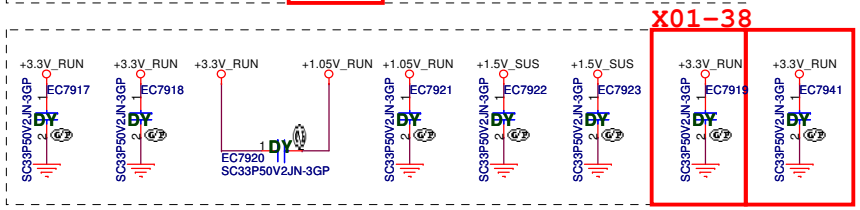
RF Cap.



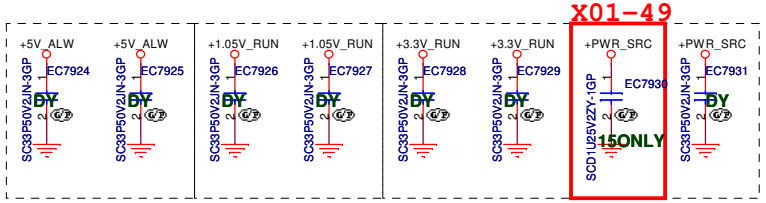
RF Cap.



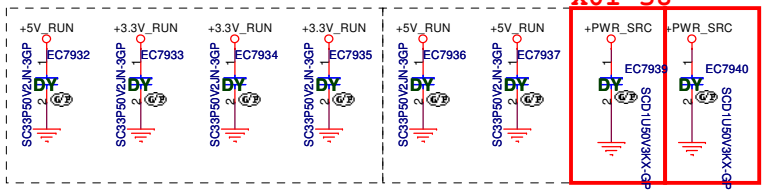
RF Cap.



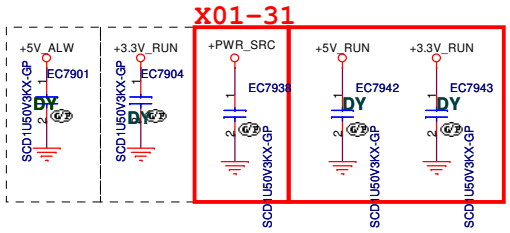
RF Cap.



RF Cap.



EMI Cap.



X01-44
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EMI Cap.

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Title: Unused Parts / EMI RF Cap.

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VERSON	DATE	NO	PAGE	Modified List	Issue Description	OWNER
X01	08/19	1	35	(remove) R3541 ; (change) R3537 to B_TPM group	LOM_TPM_EN# for B_TPM group control	EE
		2	54,64,72	(rename) F1 to FUSE5401 ; (rename) R2323 to (DY) R6402 (rename) R2320 to (DY) R7211 ; (rename) C7802 to (DY) C7226	Rename for schematic standardization Dummy R6402 and R7211 because traces already pull high.	EE
		3	27	(change) L2702, L2703 part.	Change coil for intel requirment.	EE
		4	27	(change) D2701, D2702 part.	Change diode for PSL vender.	EE
		5	9,37	(remove) TP3710 (add) R3730 for H_SKTOCC# traces.	Dell requires add CPU socket detect function.	EE
		6	37	(remove) R3738	Just for JTAG debug, remove R3738 pull high.	EE
		7	37	(change) R3703 to 130k.	Board Version (X01).	EE
		8	34,67	(add) R3411, C3409 to DY for CLK_SC_48M. (add) 0.1uF C6703 to DY for SC_DET#.	Remain AC term for SmartCard 48Mhz clock. Add 0.1uF for SC_DET#.	EE
		9	47	Update PU4701 symbol.	Correct error vender component P/N.	Power EE
	08/25	10	50	(DY) PR5007. (change) (DY) PD5001 part.	TPS51116 already built-in BST circuit. Change PD5001 to PSL vender.	Power EE
		11	42	(change) Q4207 part.	Change MOS part due to power demand.	EE
		12	54	(change) FUSE5401 part.	Use Poly-fuse instead of one time fuse.	EE
		13	54	(add) 100k R5401 to (DY) to GND.	Reserved dummy location for panel backlight control.	EE
		14	25	(change) TPM_ID1 pull high to +3.3V_RUN	Intel PCH EDS.	EE
		15	39	(change) U3901(SMSC EMC4002) to Rev.B	SMSC Version Change.	EE
		16	4,35,37	(modify) SMBus Diagram for LAN (change) KBC I2C1E group link to PCH1 and U3701 pull high +3.3V_ALW_PCH. (change) LAN SMBus from U3503 link to U3701.	Modify LAN SMBus for leakage from +3.3V_LAN to +3.3V_ALW_PCH.	EE
		17	54	(remove) R5423, R5424.	No need R pull high / down for eDP_AUX and eDP_AUX#.	EE
		18	32	(change) R3206 from 100k to 47k ohm.	For Ricoh R5U24x sequence (GBRST#).	EE
		19	32	(stuff) R2316, C2309, C2310, X2301, X2301.	Intel recommends use 25M Xtal for DCI signals.	EE
						ME

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Title: Change List (1/3)

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VERSON	NO	PAGE	ACTION	reference	Issue Description	OWNER
X01	X01-1	79	Change	H10	14U change H10 PAD size	EE
	X01-2	62	Change	U6201,U6202	change BIOS part number	EE
	X01-3	52	ADD	PG5221~PG5226	combin 1.05V_RUN and 1.05V_VTT Circuit	EE
		49	remove	+1.05V_RUN Circuit		
	X01-4	9	Change	R915-->0 ohm,R920-->0 ohm		EE
	X01-5	66	ADD	D6603,D6602	combin WWAN ,WIMAX and WLAN LED circuit	EE
			DY	R6615,Q6601,R6616,R6613		
	X01-7	58	DY	XDP1,R5808		EE
	X01-8	70	DY	LDBG1,JTAG1		EE
	X01-9	50	DY	PR5010	change discharge mode	EE
			ADD	PR5016		
	X01-10	36	Change	R3616-->1k, C360200>1U	modify TCM circuit	EE
			DY	R3606,R3607		
			remove	R3605		
	X01-11	42	Change	R4226--> 0805 size		EE
	X01-12	42,37	Change	C4208-->150P,C4211-->4700P,R3707-->10K	Tuning S3 power sequence.	EE
		52	DY	PC5211		
	X01-13	46	ADD	PR4623,PR4624	Tuning power sequence.	EE
			DY	PR4624		
	X01-14	37	Change	change 1.05V_RUN_PWRGD to test pad	combin 1.05V_RUN and 1.05V_VTT Circuit	EE
	X01-15	20	Change	R2006-->110K,R2007-->110K		EE
	X01-16	74	Change	change DK1 part number	update dock connector	ME
	X01-17	46,52 53,12	Change	PU460-->FDS8880,PU4605-->FDS6676AS,PR4602-->73K2R2F PU5203-->SI7658ADP,PC5307-->SCD068U16V2KX PR5202-->73K2R2F,PR5328-->61K9R2F PC5319-->SC1KP50V2KX,PC5318-->SC330P50V2KX R1203-->0R2J-2	Power team suggest	power-EE
		52	remove	PU5204		
	X01-18	68	ADD	R6801,R6802	EMC team suggest	EMC
	X01-19	37	modfiy	connect X3701 pin2 and pin3 to GND		EE
	X01-20	32	modfiy	R3211,R3212,R3205,R3213,R3215-->33 ohm	Tuning signal	EE
			ADD	R7116,R7117,R7118,R7119,R7120		
		71	DY	EC7106,EC7107,EC7108,EC7109		
	X01-21	39	Change	C3901-->470P,C3902-->100P		EE
	X01-22	35	ADD	U3507	add LAN EEPROM 2nd source	EE
	X01-23	47	Change	PC4729-->SCD22U25V3KX,PR4776-->6K65R2F	Power team suggest	power-EE
	X01-24	12	ADD	R1207,R1208	Power team suggest	power-EE
	X01-25	30	Change	R3014-->2K,R3025-->2K,C3029-->1KP C3030-->1KP,C3039-->1U,C3040-->1U C3035-->1U,C3036-->1U,C3031-->1KP C3032-->1KP,R3028-->2K,R3029-->2K	modify DOCK MIC and HP circuit	EE
	X01-26	73	remove	R7308,R7309	USB1.1 does not need resistors in USB pair.	EE
	X01-27	59	Change	ODD1	change dock connector	EE
	X01-28	30	Change	C3010,C3023,C3024	Factory request, create spacing.	EE
	X01-29	79	ADD	BOSS1	new part for combin pad and boss	ME
	X01-30	38,24 25	modfiy	RN3805-->100K*2,RN2401-->10K*2,RN2502-->10K*2	combin resister	EE
	X01-31	79	ADD	EC7919	EMC team suggest	EMC
	X01-32	63	modfiy	D6301	swap <Core Design>	EE

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Taipei Hsien 221, Taiwan, R.O.C.

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VERSON	NO.	PAGE	ACTION	reference	Issue Description	OWNER
X01	X01-33	23,54	ADD	EC2301,EC2302,EC5401	EMC team suggest	EMC
	X01-34	63	modfiy	EL6301	swap	EE
	X01-35	79	DY	SPR7	EMC team suggest	EMC
	X01-36	49	ADD	D6801	EMC team suggest	EMC
			modfiy	L6801,L6802		
	X01-38	79	ADD	EC7919,EC7939,EC7940,EC7941	EMC team suggest	EMC
	X01-39	35	ADD	D3502,R3548	Prevent leakage of +3.3V_RUN.	EE
	X01-40	52	ADD	PTC5203		EE
	X01-41	23	modfiy	Q2303,RN2301	14U ONLY	EE
	X01-42	71	modfiy	R7115	change R7115.2 net name to SD_MMC_CLK_L	EE
	X01-43	7,9,32 23	Change	RN3202,RN2311,RN903,RN703 RN704,RN701,RN705	change size	EE
	X01-44	79	ADD	EC7942,EC7943	EMC team suggest	
	X01-45	39	ADD	PC3901	Power team suggest	EE
		39,50	Change	R3902-->12K7R2F,R3903-->5K62R2F PR5014-->30K1R2F,PR5015-->29K4R2F		
	X01-47	22,27 24,11	Change	R2205-->10K,C2713-->1U,R2407-->8.2K,R1109-->3.3K		EE
	X01-48	24,58	Change	FAN1,RTC1 connector	ME suggest	
	X01-49	43,79 45,46	stuff	EC4301,EC7930,PC4503,PC4610,PC4615,EC7912,EC7902	EMC team suggest, 15 inch only	EMC
	X01-50	37,40 54	DY	R3734,R4006,R5425		EE
		54	stuff	R5418		
	X01-51	47	Change	PC4710,PC4709,PC4723--> 0.22U25V	Power team suggest	power-EE
	X01-52	63	DY	R6301,R6302,R6303,R6304	EMC team suggest	EMC
		63	stuff	EL6301,EL6302		

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